Development of the Advanced Deep Space Transponder

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We present the architecture and design of a new transponder to support deep-space and near-Earth missions in the post-2010 time frame. This transponder is designed to provide direct-to-Earth command and telemetry service; spacecraft-to-spacecraft command and telemetry service; direct-to-Earth navigation in the form of coherent Doppler turnaround, sequential turn-around ranging, pseudo-noise regenerative ranging, and differential one-way ranging; and spacecraft-to-spacecraft navigation in the form of coherent Doppler turnaround and one-way pseudo-noise code ranging.

I. Introduction

All JPL deep-space missions currently use transponders to provide direct-to-Earth communications and navigation services. In addition, some missions equip the transponder with an ultra-stable oscillator (USO) and use the transponder as an instrument for radio science. The transponder currently in use, the Small Deep Space Transponder (SDST),[3] manufactured at General Dynamics Decision Systems, was designed in 1992 using the technology available at the time. Over 10 years later, electronics parts used in the design are becoming obsolete, we are running out of digital application-specific integrated circuits (ASICs) from the original foundry run, and it is clear that the SDST will not be able to support new missions for more than a few more years.

As part of an effort to replace the SDST for missions scheduled in the 2010 time frame and beyond, we embarked upon a research and technology development task in 2003 to put together an architecture for the next-generation transponder and to develop the digital signal-processing capabilities needed by future missions. In this article, we will discuss our progress on this ongoing task. We will present our design rationale, the functional and performance requirements on which we are basing our architecture, some signal-processing design analysis, and experimental results we have achieved to date with a prototype radio-frequency front end and digital development platform.

II. Design Rationale

In the formulation of the architecture of the Advanced Transponder, we were guided by the design goals enumerated in the following subsections. In all cases, we have tried to make maximum use of the design heritage of the Cassini Deep Space Transponder (DST),[4] the Small Deep Space Transponder (SDST), and the JPL Spacecraft Transponding Modem (STM) [1], which unfortunately was not completed.

A. Preservation of Function and Performance

Our starting point in this effort was that we would not reduce the functionality or degrade the performance of the existing SDST. Rather, all new functionality would serve to enhance performance while preserving the specifications to which current missions are designing. In the process of developing this design, we have come upon a few areas in which we may want to make compromises. These areas are listed here and described in more detail in later sections:

(1) Radio Science: The downlink carrier stability requirements for radio science are design drivers and may be difficult to meet given our new frequency-agile front-end architecture. If we find that we cannot meet these requirements with our generic architecture, our modular design will allow us to develop a front-end module specifically for radio science that meets the stability requirements at the expense of some tuning-range capability. In other words, radio science may require a dedicated front-end module, which can be developed for missions specifically requiring that function.

(2) Downlink Telemetry Encoding: The SDST provides a wide range of convolutional encoding mode options although the only options ever used in flight have been 7-1/2 and 15-1/6 non-return-to-zero-level (NRZ_L). We are considering eliminating the other convolutional encoding options, especially because we will be implementing turbo coding as a downlink option.

B. Reduction of Power, Weight, and Manufacturing Cost

The current SDST (in the Mars Exploration Rover 8.4-GHz (X-band) downlink-only configuration) weighs about 2.6 kg, draws about 14 W while transmitting,[5] and involves large recurring engineering production costs, largely because of hand tuning of a large number of RF components and the use of relatively low-yield RF multi-chip modules (MCMs). Our approach in this effort has been to push much of the functionality into the digital realm, eliminating secondary analog downconversion stages, and simplifying the RF architecture. We also have identified radio frequency integrated circuits (RFICs) or monolithic microwave integrated circuits (MMICs) that either are in development or could be developed that would allow elimination of the multi-chip modules that account for much of the touch labor, board area, and design risk in the SDST. With these changes, we are anticipating at least a 50 percent reduction in mass, power, and unit production cost.

C. Support of Spacecraft Crosslinks as well as Direct-to-Earth Links

A major enhancement to the functionality of the DST, SDST, and STM is the addition of spacecraft crosslink, or spacecraft-to-spacecraft, communications and navigation service. As future solar system exploration programs send multiple spacecraft to a single target or fly constellations of spacecraft, we will need to support data relay and exchange of information between multiple spacecraft. In addition, as we require greater landing precision, we need to rely on assets in orbit around a target to enhance navigation by providing Doppler measurement and pseudo-noise (PN) ranging sessions with an approaching lander

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[4] *Deep Space Transponder Specification*, JPL FM 513778 (internal document), Jet Propulsion Laboratory, Pasadena, California, March 1994.

[5] *Mars Exploration Rover Hardware Review/Certification Requirements (HRCR) 1001*, MER 420-3-480 (internal document), Jet Propulsion Laboratory, Pasadena, California, February 2002.

in directions orthogonal to the Earth–probe line of sight. We have incorporated this functionality into the architecture of the Advanced Transponder.

D. Increase in Data Throughput

To support the increased data volumes of future missions, our goal is to extend the downlink telemetry rate to 100 Mb/s, which would be available as a quadrature phase-shift keying (QPSK) modulation mode at 32-GHz (Ka-band) downlink frequencies (since the X-band allocation does not support this wide of a bandwidth). To support large software uploads and data relay services, we will extend the uplink data rate capability to 256 kb/s, up from the 2 kb/s maximum rate supported by the SDST and STM.

E. Incorporation of Key Telecommunications–Avionics Functions

Another goal behind the development of this architecture is the incorporation into the transponder of key telecommunications functions that have traditionally been performed in avionics:

(1) Command Code Block Processing. The synchronized uplink bit stream is scanned for the 0xEB90 start sequence, and command code blocks are decoded, validated using the cyclic redundancy check codes, and then transferred to avionics as a validated code block.

(2) Hardware Command Decoding. As part of the command decoding process, virtual-channel-0 commands are identified, and the indicated latching relay is set or cleared.

(3) Downlink Turbo and Reed–Solomon Encoding. Data are transferred from avionics to the transponder as a complete frame. The transponder then performs Reed–Solomon plus convolutional encoding or turbo encoding on the full frame as requested and then downlinks the frame.

The result of these architectural changes, as compared to the SDST baseline, is that the interface between the transponder and avionics becomes a frame-level rather than a bit-level interface. This eliminates the need for synchronous data–clock–lock interfaces and allows the command and telemetry paths to share a single high-rate interface with the transponder mode control and data interface. This change also eliminates the need for special Reed–Solomon and turbo encoding software and hardware, as well as hardware command decoder hardware, on the avionics side, freeing up spacecraft system resources that can be applied instead to science data processing.

F. Built-In Redundancy and Modular Design

In order to simultaneously support a direct-to-Earth (DTE) link and a spacecraft crosslink, and to build in functional redundancy, we have targeted a modular architecture allowing interchangeability between the DTE and crosslink baseband digital processors, as well as between optional RF front ends operating at 2.2 GHz (S-band), 8.4 GHz (X-band), or 32 GHz (Ka-band).

In this design, two identical baseband processors operate in parallel, one targeted for DTE and the other for crosslink. At the time of manufacture, two switchable RF front-end modules are selected for each baseband processor. For example, an X-band and a Ka-band module might be selected for the DTE channel, and a normal and an inverted S-band module might be selected for the crosslink channel. In the case of a DTE channel failure, the S-band crosslink channel, which supports identical digital signal processing, could be used for backup communications with the Deep Space Network (DSN). A more detailed look at this architecture is presented in Section III.

G. Design of a Frequency-Agile Front End

Another key goal in this development is to provide a frequency-agile front end that can be tuned in flight to cover all channels in the DSN band allocation. The current SDST is assigned a channel frequency at time of manufacture by the selection of a crystal oscillator and other frequency-specific parts. This

makes the sharing of spare units between projects particularly difficult if they are operating with different frequency assignments.

The challenge in implementing this tunability is that the required reduction in the quality factor (Q) of the dielectric resonance oscillator phase-locked loop (DRO-PLL) could degrade the phase noise performance of the carrier-tracking and downlink synthesis loops. However, preliminary laboratory work with the STM DRO [2] design indicates that the Q of the DRO is not the primary contributor to the phase noise, and we do not see significant degradation due to the increased coupling. These results are presented later in this article. In addition, the narrow bandwidth of the digital carrier-tracking loop can be maintained in order to preserve the low uplink signal detection threshold.

H. Addition of New Signal-Processing Functions

Finally, another driving goal is to incorporate enhanced digital signal processing in order to provide additional functionality over what the current SDST provides. New functions included in this design include the following:

(1) Pseudo-Noise (PN) Regenerative Ranging. By synchronizing to and regenerating a pseudo-noise ranging signal onboard, we can dramatically improve ranging performance. For a typical Mars mission, this improvement is estimated to be about 17 dB [3].

(2) Crosslink PN Ranging. For spacecraft-to-spacecraft navigation, the same PN correlator used for direct-to-Earth navigation can be applied to measuring the phase of an arriving PN signal from another spacecraft. With exchange of clock information over the communications channel, these data can be used to calculate range information. At the 1-MHz chip rate used for DTE navigation, and using a 20-MHz processing clock, we expect to achieve a resolution of less than 20 m. It also may be possible to get sub-clock-edge resolution by integration over many clock cycles.

(3) Quadrature Phase-Shift Keying (QPSK) Downlink Modulation. We have incorporated both a linear phase modulator and a QPSK modulator into this design to support high-rate signaling on the downlink. Note that the SDST to be flown on the Mars Reconnaissance Orbiter (MRO) has also included QPSK modulation as an upgrade in the form of an additional field programmable gate array (FPGA).

(4) Phase-Shift Keying (PSK) Command Demodulator. In order to receive high-rate uplink, we have incorporated a PSK uplink demodulator in addition to the traditional command detection unit (CDU) from the SDST. The PSK demodulator enables crosslink communications by providing a receiver that is compatible with the PSK downlink modulation format used by the SDST and by the Advanced Transponder.

III. Transponder Architecture

Our goals in this research effort were to push the RF–digital boundary further toward the digital side, to create a modular and interchangeable front-end design, to identify and specify RF components to be procured or developed, and to provide flexibility and programmability in the digital signal processing. This section provides a detailed description of the architecture developed during the first year of this research task.

A. Modular Functional Partitioning

The key aspect of the front-end design is the identification of configurable RF modules that can be combined at time of manufacture with the same digital back end in order to provide mission-specific performance and functional redundancy. Three key frequency bands were identified for development: Ka-band, X-band, and S-band. Ka-band, operating at 34 GHz and 32 GHz for uplink and downlink,

respectively, is an enabling communication band for future high-data-rate missions requiring more data bandwidth than can be supported at X-band. X-band, at 7.1 GHz and 8.4 GHz for uplink and downlink, respectively, provides backward compatibility for current missions, is fully supported by all Deep Space Network stations, and provides good emergency-rate downlink and practical low-gain performance for missions that lose or do not have the capability to accurately point a Ka-band antenna. S-band, at 2.1 GHz and 2.2 GHz for uplink and downlink, respectively, is primarily used in this architecture as a relay channel for crosslink spacecraft-to-spacecraft communication. In addition, because the DSN still supports S-band communications, this channel can be used as a functional backup for direct-to-Earth communications.

The architecture we have developed allows for the simultaneous operation of two separate two-way coherent front ends. In addition, each of these two channels can be switched to one of two separate RF modules, providing four available front ends, two of which can be used simultaneously. Figure 1 provides an overview of this front-end architecture.

The digital processing back ends for the DTE link and crosslink channels are identical and can be used interchangeably for either function. This provides built-in functional redundancy to increase reliability and potentially eliminate the need for some missions to fly two transponders.

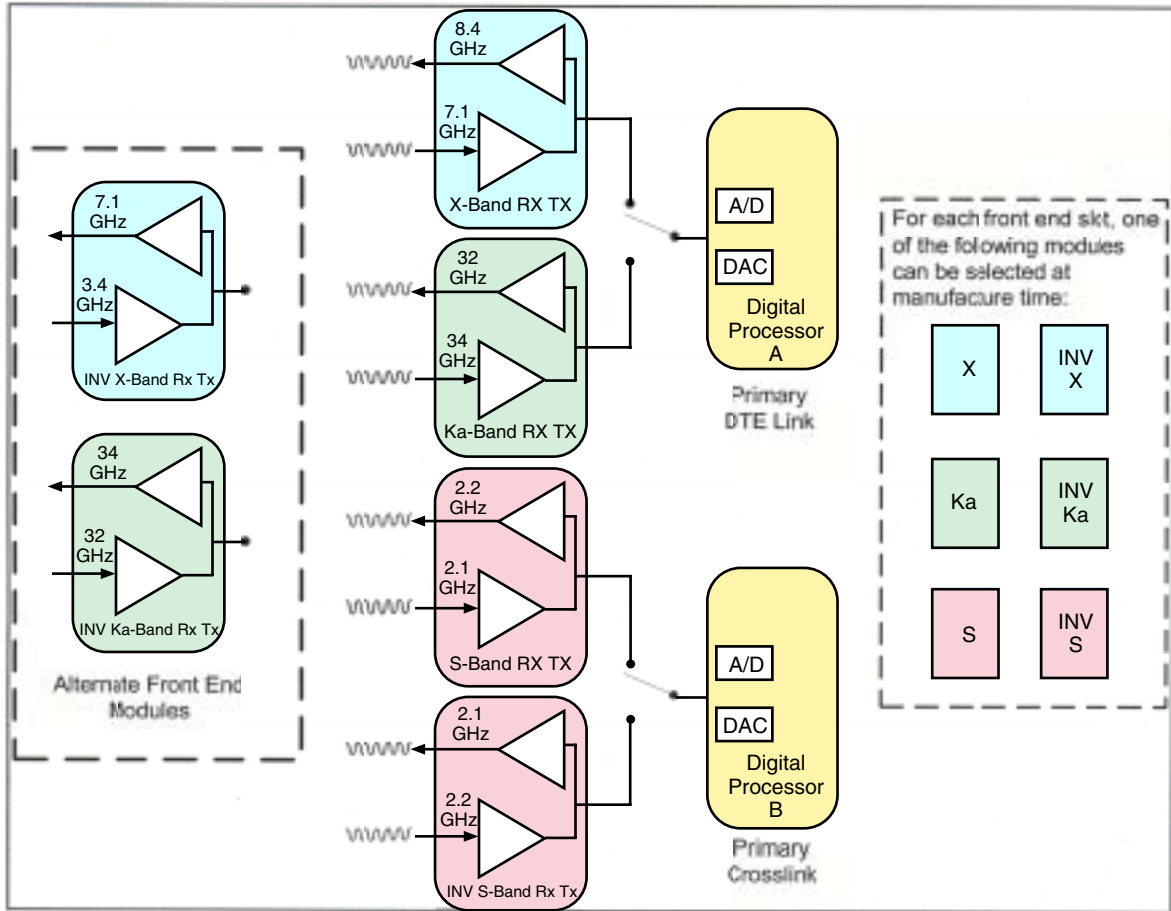Fig. 1.   Modular front-end architecture, illustrating dual parallel digital processors and four selectable RF front-end modules, each of which can be configured at manufacture time to one of six possible front ends: S-band, X-band, or Ka-band, or channel-inverted S-band, X-band, or Ka-band. The most common configuration (X-band and Ka-band for DTE and S-band and inverted S-band for crosslink) is shown.

B. RF Front-End Architecture

In addition to providing manufacture-time configurability, the architecture we have developed also will allow for in-flight tuning of the primary RF uplink and downlink frequencies to cover the full Deep Space Network band allocation. This tunability is achieved through the development of a dielectric resonance oscillator (DRO) with dual varactor coupling. One varactor is relatively lightly coupled to provide fine tuning for loop locking and tracking, while the other is tightly coupled to allow coarse frequency tuning by means of a programmable digital-to-analog converter (DAC) driven by the digital processor FPGA. Details of the DRO development are presented in subsequent sections. In this section, the detailed discussion of the architecture continues with a description of how the dual-varactor DRO is incorporated into the transponder architecture to allow tunability while maintaining a single digital processor architecture and supporting the Consultative Committee for Space Data Systems (CCSDS) coherent turn-around ratios for each band allocation. Table 1 summarizes the required turn-around ratios for the S-band, X-band, and Ka-band deep-space allocations [4].

The architecture of each of the front-end modules is based on a phase-locked loop which phase locks the DRO to a crystal reference oscillator. The same reference oscillator (at $160 * f0$, where $f0 = 9.45$ MHz) can be used for all of the front-end modules. Tunability is achieved by mixing the reference oscillator frequency with an offset frequency synthesized in the digital processor using a numerically controlled oscillator (NCO), also derived from the reference oscillator. By careful selection of the frequency scheme, all RF modules will operate at the same intermediate frequency (IF), at the same uplink sample rate, and with the same downlink NCO synthesizer tuning range. Figures 2 through 13 illustrate in detail how this design is achieved for each frequency band.

The block diagrams of the various front ends show that essentially the same architecture can be preserved across all the communication bands and that a common digital processor can be used as the back end for any selected module. One complexity is that the established turn-around ratios allow for simple downconversion and synthesis, but when the ratio is reversed for the crosslink application, the resulting downconversion and upconversion scheme becomes somewhat awkward and requires the addition of another mixing stage for the inverted channels. In order to reduce the complexity of the inverted channel architecture, the IF is adjusted from 13 f0 to 15 f0. Using the same sampling clock in the digital processor results in a baseband band reversal in the digital processor. This is easily remedied in the FPGA by multiplication of the analog-to-digital converter (ADC) samples by a $+1, +1, -1, -1, \cdots$ sequence. Whenever the selection of an inverted channel is commanded, this baseband correction sequence is applied.

Table 1. DSN-specified coherent turn-around ratios for S-band, X-band, and Ka-band allocations.

DSN frequency band	Uplink/downlink turn-around ratio
S	221/240
X	749/880
Ka	3557/3344

X-Band Receiver (880/749)

fb =	9.45	MHz	
DSN Chan	UL RF (MHz)	fd (MHz)	Rcvr DAC (MHz)
3	7149.60	0.10	1.55543
10	7157.69	0.11	1.73130
20	7169.25	0.12	1.98261
32	7183.12	0.14	2.28413
33	7184.27	0.14	2.30913
37	7188.90	0.15	2.40878

Fig. 2. X-band receiver front end, showing downconversion of 749 f0 to an IF of 13 f0.

X-Band Downlink Synth (880/749)

Turnaround Ratio:
DL/UL = 880/749

X-Band			
fb =	9.45	MHz	
DSN Chan	DL RF (MHz)	fd (MHz)	Rcvr DAC (MHz)
3	8400.06	0.095522727	1.536363636
10	8409.57	0.108329545	1.701272727
20	8423.15	0.121761364	1.948181818
37	8446.23	0.147988636	2.367818182

Fig. 3. X-band downlink synthesis of 880 f0 carrier.

Inverted Turnaround Ratio:
DL/UL = 749/880

X-Band			
fb =	9.45	MHz	
DSN Chan	RX RF (MHz)	fd (MHz)	Rcvr DAC (MHz)
3	8400.06	0.095522727	1.554862052
10	8409.57	0.106329545	1.730774566
20	8423.15	0.121761364	1.981985318
37	8446.23	0.147988636	2.408870613

Fig. 4. Inverted X-band receiver downconverting 880 f0 uplink to an IF of 15 f0.

INVERTED X-Band Downlink Synth
(749/880)

Turnaround Ratio:
DL/UL = 749/880

X-Band			
fb =	9.45	MHz	
DSN Chan	DL RF (MHz)	fd (MHz)	Synth DAC (MHz)
3	7149.6	0.09552737	0.362109479
10	7157.69	0.106329408	0.425313752
20	7169.25	0.12176235	0.487049099
37	7188.9	0.14799733	0.591969319

Fig. 5. Inverted X-band downlink synthesis of 749 f0 carrier.

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Ka-Band Receiver Front End: 3344/3597 DL/UL

Turnaround Ratio:
DL/UL = 3344/3597

Ka-band			
fb =	9.45	MHz	
DSN Chan	UL RF (MHz)	fk (MHz)	Rcvr DAC (MHz)
1	34024.15	0.092438143	1.484375
10	34074.11	0.106327495	1.707410714
30	34185.13	0.137192105	2.200035714
42	34251.74	0.155710314	2.500401786

Fig. 6. Ka-band receiver front end downconverting 3597 f0 uplink to an IF of 13 f0.

Ka-Band Downlink Synth

Turnaround Ratio:
DL/UL = 3344/3597

Ka-Band			
fb =	9.45	MHz	
DSN Chan	DL RF (MHz)	fk (MHz)	Rcvr DAC (MHz)
1	31909.91	0.092437201	1.478895215
10	31956.36	0.106327751	1.701244019
30	32059.57	0.137191986	2.19507177
42	32121.49	0.155708732	2.491339713
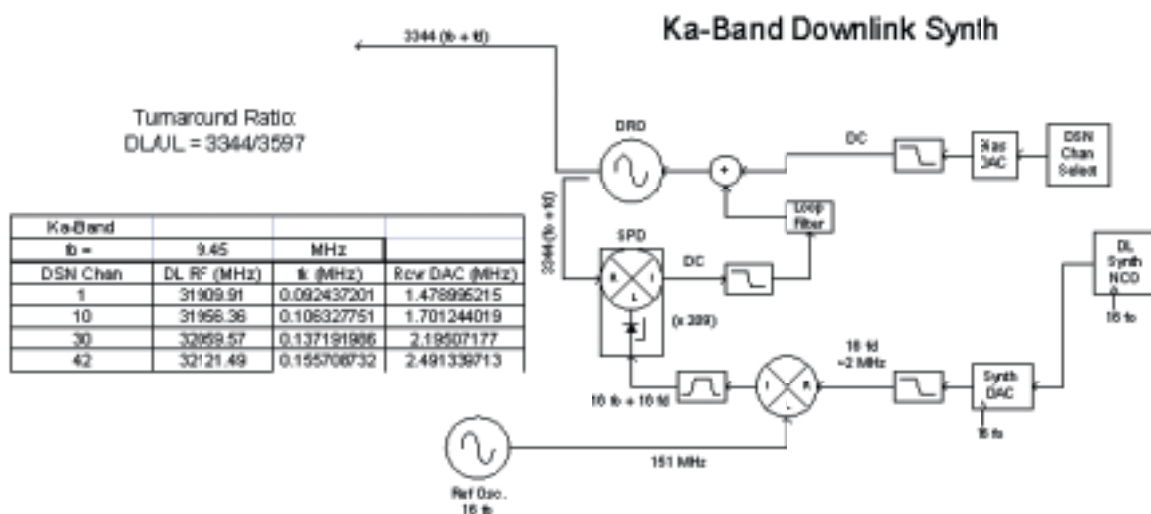
Fig. 7. Ka-band downlink synthesis of 3344 f0 carrier.

INVERTED Ka-Band Receiver
(3597/3344)

Inverted Turnaround Ratio:
DL/UL = 3597/3344

X-Band			
fo =	9.45	MHz	
DSN Chan	RX RF (MHz)	fd (MHz)	Rcvr DAC (MHz)
1	31909.91	0.092437201	1.485659357
10	31956.36	0.106327751	1.708909582
30	32059.57	0.137191966	2.204982451
42	32121.49	0.155706732	2.502985335

Fig. 8. Inverted Ka-band receiver downconverting 3344 f0 uplink to 15 f0.

INVERTED Ka-Band Downlink Synth
(3597/3344)

Turnaround Ratio:
DL/UL = 3597/3344

Ka-Band			
fo =	9.45	MHz	
DSN Chan	DL RF (MHz)	fd (MHz)	Synth DAC (MHz)
1	34324.15	0.092438143	0.369752572
10	34374.11	0.106327495	0.425305981
30	34485.13	0.137192105	0.548769418
42	34551.74	0.155710314	0.622841257

Fig. 9. Inverted Ka-band downlink synthesis of 3597 f0 carrier.

S-Band Receiver (240/221)

Turnaround Ratio:
DL/UL = 240/221

S-Band			
f0 =	9.45	MHz	
DSN Chan	UL RF (MHz)	f0 (MHz)	Rcvr DAC (MHz)
5	2110.24	0.096597285	1.676153846
10	2111.95	0.106334842	1.807692308
20	2115.36	0.121764706	2.07
27	2117.75	0.132579186	2.253846154

Fig. 10. S-band uplink downconversion of 221 f0 uplink to an IF of 13 f0.

S-Band Downlink Synth (240/221)

Turnaround Ratio:
DL/UL = 240/221

S-Band			
f0 =	9.45	MHz	
DSN Chan	DL RF (MHz)	f0 (MHz)	Rcvr DAC (MHz)
5	2291.67	0.098825	1.578
10	2293.52	0.106333333	1.701333333
20	2297.22	0.12175	1.948
27	2299.81	0.132541667	2.120666667

Fig. 11. S-band downlink synthesis of 240 f0 carrier.

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INVERTED S-Band Receiver (221/240)

Inverted Turnaround Ratio:
DL/UL = 221/240

S-Band			
fo =	9.45	MHz	
DSN Chan	RX RF (MHz)	fd (MHz)	Rcvr DAC (MHz)
5	2291.82	0.098825	1.8832
10	2293.52	0.106333333	1.814755556
20	2297.22	0.12175	2.077866667
27	2299.86	0.132541667	2.262044444

Fig. 12. Inverted S-band receiver downconverting 240 f0 uplink to 15 f0.

INVERTED S-Band Downlink Synth (221/240)

Turnaround Ratio:
DL/UL = 221/240

S-Band			
fo =	9.45	MHz	
DSN Chan	DL RF (MHz)	fd (MHz)	Synth DAC (MHz)
5	2110.24	0.098597285	0.39438914
10	2111.95	0.106334842	0.425339367
20	2115.36	0.121764706	0.487058824
27	2117.75	0.132579186	0.530316742

Fig. 13. Inverted S-band downlink synthesizer generating 221 f0 carrier.

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C. Digital Processing Architecture

As illustrated in the block diagrams of the RF front-end modules, uplink downconversion proceeds in a single step to an IF of 13 f0 (or 15 f0). The DRO-PLL tracking loop is actually closed inside the digital processor using an NCO to generate an offset frequency to mix with the reference oscillator and lock the DRO loop.

The 13 f0 IF is digitized by an analog-to-digital converter clocked at 4 f0 to produce quadrature baseband in-phase (I) and quadrature-phase (Q) samples. In lock, the Q samples have zero carrier component, and the I samples will be integrated and compared to a threshold to determine lock status. The uplink ranging and command modulation will appear on the Q channel, which will be integrated and routed to the standard command detection unit, the high-rate PSK command decoder, and to the ranging processor.

The I and Q samples are used to generate a total signal strength estimate $[\sqrt{(I^2 + Q^2)}]$, which is used for coherent automatic gain control (AGC) to scale the I samples driving a second-order tracking-loop filter, the output of which controls the frequency of the receiver NCO, closing the receiver tracking loop.

The frequency and phase of the receiver NCO is digitally locked to a second NCO, which is used to drive the downlink synthesis loop. This downlink offset frequency reference is generated by direct digital synthesis and applied to the sampling phase detector to lock the downlink DRO-PLL synthesis loop.

Figure 14 provides a block diagram of the digital tracking and downlink synthesis signal processing. Note that the receiver NCO and synthesis NCO are shown driving a sine look-up table and digital-to-analog converter (DAC). In Section VII, experimental data are presented to illustrate a novel method by which the DAC and subsequent mixing stages may be eliminated by digital multiplication and direct digital drive of the sampling phase detector.

IV. RF Component Specifications and Analysis

A. X-Band Receiver and Transmitter RF Components

The major RF components for the X-band transponder include a pre-select filter, a low-noise amplifier (LNA), a gain amplifier, an image reject mixer (IRM), an IF amplifier, a multi-channel receiver/transmitter DRO and voltage-controlled oscillator, a linear phase modulator, and a QPSK modulator. The specifications for these components are given in Tables 2 through 9. All of the components, with the exception of the pre-select filter, are based on monolithic microwave integrated circuit (MMIC) technology.

1. Low-Noise Amplifier. Low-noise amplifier MMICs with a 0.8-dB noise figure and a 20-dB gain are commercially available.

2. IRM, VCO, Phase Modulator, QPSK Modulator. The image reject mixer (IRM), voltage-controlled oscillator (VCO), phase modulator, and QPSK modulator were developed by Hittite Microwave Co., under contract with the NASA Small Business Innovation Research (SBIR) program. The metal semiconductor field effect transistor (MESFET) used in these designs is a standard 0.5-μm depletion-mode MESFET from TriQuint Semiconductor, Inc. Two iterations of design, computer-aided design (CAD) analysis, and fabrication were used to optimize the performance of the MMIC chips.

3. VCO MMIC. The negative resistance VCO MMIC chip incorporates a negative resistance oscillator along with a buffer amplifier. This VCO has been simulated using CAD tools to have large negative resistance over the frequency range of 7 GHz to 8.5 GHz.

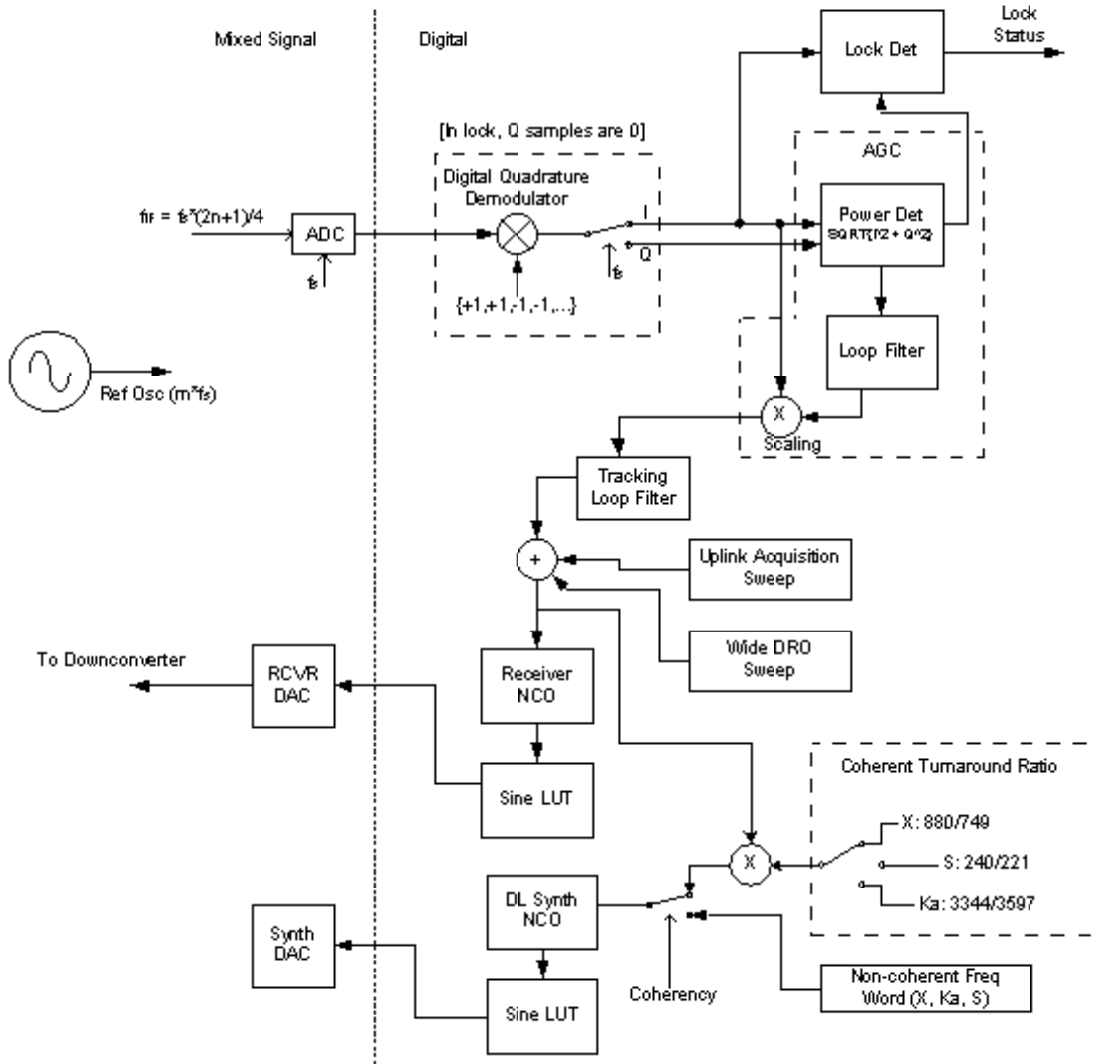Digital Carrier Tracking and Downlink Synthesis

Fig. 14. Digital tracking and synthesis loop architecture.

4. Linear Phase Modulator. The MMIC phase-shifter chip incorporates a four-stage reflection phase shifter with Lange couplers and MESFET varactors to provide a phase deviation of ±100 deg with better than 8 percent linearity in the 8-GHz to 8.5-GHz range.

We are currently planning to procure an S-level MMIC phase modulator with an added internal amplifier, and a QPSK MMIC modulator.

5. DRO. The multi-channel DRO is under development at present; this development needs to be continued next year to finalize the design and breadboard evaluation. The DRO-PLL covers the DSN range of 50 MHz at X-band. The task includes the new design of the breadboard, widening the free-running DRO tuning frequency range to 50 MHz, design of swept-lock control and PLL circuits, fabrication of the circuits, and test and evaluation of the breadboard. The DRO-PLL will be evaluated for channel-placing and -locking capabilities and phase noise performance of the locked DRO.

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Table 2. Multi-channel receiver/transmitter DRO specification.

DRO parameter	Specification
X-band RF frequency range:	
X-band receive DRO frequency range	$\sim$7019 MHz to 7069 MHz
X-band transmit DRO frequency range	$\sim$8400 MHz to 8450 MHz
Course electronic tuning range (receiver)	TBD: $\sim$7039 MHz $\pm$ 25 MHz
Fine tuning range (PLL capture range)	$\pm$2 MHz
Tuning linearity	$\pm$10% or better
Output power level	+10 dBm $\pm$ 1.0 dB
Free-running DRO SSB phase noise	< -50 dBc/Hz at 1 KHz off carrier
Frequency stability versus temperature	$\pm$2 ppm/deg C max
Frequency pushing ($\pm$5% Vdc)	100 kHz max
Frequency pulling (2:1 voltage standing wave ratio (VSWR) all phases)	100 kHz max
Harmonics	< -33 dBc
Spurious signals	< -80 dBc
Operating temperature range	-55 deg C to +75 deg C
Output impedance	50 $\pm$ 5 ohms, nominal
DC bias current at +5V DC	30 mA
Course electronic tuning control voltage	+3 V $\pm$ 2 V max
Fine tuning control voltage	+3V $\pm$ 2 V max

Table 3. Pre-select filter specification.

Pre-select filter parameter	Specification
RF frequency range	7148 to 7195 MHz
Insertion loss	$<$0.4 dB
Gain flatness	$\pm$0.1 dB, nominal
0.25 dB bandwidth	7170 $\pm$ 22 MHz
3 dB bandwidth	7170 $\pm$ 25 MHz
Input impedance	50 $\pm$ 5 ohms, nominal
Input VSWR	1.2:1
Output impedance	50 $\pm$ 5 ohms, nominal
Output VSWR	1.5:1
Operating temperature range	-55 deg C to +75 deg C

Table 4. Receiver LNA specification.

LNA parameter	Specification
RF frequency range	7148 to 7195 MHz
Gain	15 dB
Gain flatness	±0.1 dB, nominal
Noise figure	0.8 dB max at 25 deg C
1 dB compression [$P_{1\mathrm{dB}}$]	+10 dBm
Input impedance	50 ± 5 ohms, nominal
Input VSWR	1.2:1
Output impedance	50 ± 5 ohms, nominal
Output VSWR	1.5:1
Power consumption	<50 mW
Operating temperature range	−55 deg C to +75 deg C

Table 5. Mixer input gain amplifier specification.

Gain amplifier parameter	Specification
RF frequency range	7148 to 7195 MHz
Gain	∼22 dB
Gain flatness	±0.25 dB
Noise gigure	3 dB max at 25 deg C
1 dB compression [$P_{1\mathrm{dB}}$]	+10 dBm
Image rejection	−30 dBc
Input impedance	50 ± 5 ohms, nominal
Input VSWR	<1.5:1
Output impedance	50 ± 5 ohms, nominal
Output VSWR	<1.5:1
Power consumption	<100 mW
Operating temperature range	−55 deg C to +75 deg C

Table 6. Image reject mixer (IRM) specification.

IRM parameter	Specification
RF frequency range	7145 to 7200 MHz
LO frequency range	~7019 MHz to 7069 MHz
IF frequency	110 to 130 MHz
Conversion loss	<8 dB
SSB noise figure	<8 dB
LO power level	<16 dBm
Image rejection	−30 dBc min
Isolation LO to RF (leakage)	>20 dB
Isolation LO to IF (leakage)	>30 dB
Impedance (RF, LO, and IF ports)	50 ± 5 ohms, nominal
VSWR (RF, LO, and IF ports)	<1.5:1
RF input at 1 dB compression [$P_{1\mathrm{dB}}$]	+13 dBm
Power consumption	0 mW
Operating temperature range	−55 deg C to +75 deg C

Table 7. Intermediate frequency amplifier (IF-Amp) specification.

IF-Amp parameter	Specification
RF frequency range	110 to 130 MHz
Gain	25 dB
Gain flatness	± 0.5 dB, nominal
Noise figure	6 dB max at 25 deg C
1 dB compression [$P_{1\mathrm{dB}}$]	+10 dBm
Impedance (input and output ports)	50 ± 5 ohms, nominal
VSWR (input and output ports)	1.2:1
Power consumption	<100 mW
Operating temperature range	−55 deg C to +75 deg C

Table 8. Design specifications for the X-band MMIC linear phase modulator.

Parameter	Specification
Design frequency range	8400 to 8450 MHz
Modulation bandwidth at the mod-input port:	
−0.25 dB bandwidth	±30 MHz
−3 dB bandwidth	±100 MHz min
Linear phase shift	±2.5 rad peak
Modulation linearity	±8% (best straight line) to ±2.5 rad peak
Modulation sensitivity	>120 deg/V, peak
Modulation voltage range	2 to 5 V
Insertion loss	10 dB max
Insertion loss flatness	±0.5 dB max over tuning range
	±1 dB max over tuning and temperature range
RF port return loss	15 dB min
RF power (1 dB compression)	+10 dBm
DC power consumption	50 mW
Design temperature range	−55 deg C to +75 deg C

Table 9. Design specifications for the X-band MMIC QPSK/BPSK modulator.

Parameter	Specification
Design frequency range	8400 to 8450 MHz
Data rate	1 kb/s to 20 Mb/s max
RF output bandwidth	±150 MHz min
Phase balance	±4 deg
Amplitude balance	±0.6 dB
Carrier suppression	−30 dBc min
RF insertion loss	−12 dB max
RF port return loss	−15 dB min
RF power input for 1 dB compression	+15 dBm
Differential drive voltage	0 and +2V (goal)
RF interface	Ground–signal–ground (GSG) pads:
	100 μm GSG pads on 150 μm min
DC–signal interface	100 μm × 100 μm pads min
Thermal–mechanical interface	Metalized (gold) back side
Operating temperature range	−5 deg C to +40 deg C
Acceptance temperature range	−50 deg C to +40 deg C

B. Ka-Band Receiver and Transmitter Microwave Components

The specifications for the Ka-band components, including the pre-select filter, LNA, multi-channel Ka-Band DRO, linear phase modulator, and QPSK modulator, are given in Tables 10 through 14.

1. LNA. Ka-band LNA MMICs with a 2-dB noise figure and a 15-dB gain are commercially available.

2. Linear Modulator and Phase Shifter. Voltage-controlled active phase shifting will be used to design linear phase modulators and phase shifters. The present technology utilizes a Ka-band MMIC varactor-based design to provide the linear phase shifting function. The Ka-band MMIC phase shifter, QPSK modulator, and x4 multiplier are currently under development at the Applied Physics Laboratory (APL) for JPL/NASA. The MMICs chips to be developed represent the core Ka-band chips needed for the next generation of advanced transponders.

The desired functional specification for the Ka-band MMIC phase shifter is shown in Table 13. The main specification goal is to provide a phase shift of ± 2.5 rad with linearity better than ± 8 percent with low amplitude insertion loss variation of ± 0.5 dB over the tuning range. The phase shifter also is used in the phased array application.

The main objective of the QPSK modulator is to provide the 1-kb/s to 100-Mb/s data-rate capability future Mars and other space missions require to transmit science data and video signals to Earth. A digital binary phase-shift keying (BPSK)/QPSK modulator at Ka-band is preferred over X-band because of channel bandwidth constraints and performance limitations at X-band.

Table 10. Multi-channel receiver/transmitter Ka-DRO specification.

DRO parameter	Specification
X-band RF frequency range:	
X-band receive DRO frequency range	$\sim$34 GHz (TBD)
X-band transmit DRO frequency range	$\sim$32 GHz (TBD)
Course electronic tuning range (receiver)	TBD: $\sim$34 MHz $\pm$ 100 MHz
Fine tuning range (PLL capture range)	± 2 MHz
Tuning linearity	$\pm 10\%$ or better
Output power level	$+10$ dBm $\pm$ 1.0 dB
Free-running DRO SSB phase noise	< -50 dBc/Hz at 1 kHz off carrier
Frequency stability versus temperature	± 2 ppm/deg C max
Frequency pushing ($\pm 5\%$ Vdc)	100 kHz max
Frequency pulling (2:1 VSWR all phases)	200 kHz max
Harmonics	< -33 dBc
Spurious signals	< -80 dBc
Operating temperature range	-55 deg C to $+75$ deg C
Output impedance	50 ± 5 ohms, nominal
DC bias current at $+5$V DC	100 mA
Course electronic tuning control voltage	$+3$ V $\pm$ 2 V max
Fine tuning control voltage	$+3$V $\pm$ 2 V max

Table 11. Ka-band pre-select filter specification.

Pre-select filter parameter	Specification
RF frequency range	$\sim$34 GHz (TBD)
Insertion loss	<1.0 dB
Gain flatness	$\pm$0.2 dB, nominal
0.25 dB bandwidth	34 GHz $\pm$ 100 MHz
3 dB bandwidth	34 GHz $\pm$ 200 MHz
Input impedance	50 $\pm$ 5 ohms, nominal
Input VSWR	1.2:1
Output impedance	50 $\pm$ 5 ohms, nominal
Output VSWR	1.5:1
Operating temperature range	-55 deg C to $+75$ deg C

Table 12. Ka-band receiver LNA specification.

LNA parameter	Specification
RF frequency range	$\sim$34 GHz (TBD)
Gain	15 dB
Gain flatness	$\pm$0.2 dB, nominal
Noise figure	2.0 dB max at 25 deg C
1 dB compression [$P_{1\text{dB}}$]	$+10$ dBm
Input impedance	50 $\pm$ 5 ohms, nominal
Input VSWR	1.2:1
Output impedance	50 $\pm$ 5 ohms, nominal
Output VSWR	1.5:1
Power consumption	<100 mW
Operating temperature range	-55 deg C to $+75$ deg C

Table 13. Design specifications for the Ka-band MMIC linear phase modulator.

Parameter	Specification
Design frequency range	31.8 to 33.0 GHz
Channel 19: 3344f1 frequency (Channel 19, f1 = 9.570216 MHz)	32.0028 GHz
Modulation bandwidth at the mod input port:	
-0.25 dB bandwidth	±60 MHz
-3 dB bandwidth	±150 MHz min
Linear phase phift	±2.5 rad peak
Modulation linearity	$\pm8\%$ (best straight line) to ±2.5 rad peak
Modulation sensitivity	>120 deg/V, peak
Modulation voltage range	2 to 5 V
Insertion loss	10 dB max
Insertion loss flatness	±0.5 dB max over tuning range ±1 dB max over tuning and temperature range
RF port return loss	15 dB min
RF power (1 dB compression)	+10 dBm
DC power consumption	100 mW
Design temperature range	-55 deg C to +75 deg C

Table 14. Design specifications for Ka-band MMIC QPSK/BPSK modulator.

Parameter	MMIC QPSK modulator specification
Design frequency range	31.8 to 33.0 GHz
Channel 19: 3344f1 frequency (Channel 19, f1 = 9.570216 MHz)	32.0028 GHz
Data rate	1 kb/s to 100 Mb/s max
RF output bandwidth	±600 MHz
Phase balance	±5 deg
Amplitude balance	±0.5 dB
Carrier suppression	30 dBc min
RF insertion loss	15 dB max
RF port return loss	15 dB min
RF power input for 1 dB compression	+10 dBm
Drive voltage and current	<5 V, TBD
Design temperature range	-55 deg C to +75 deg C

C. S-Band Components

The required S-band RF components are commercially available, and no new development is necessary at this time.

D. Future Technology Developments

The following tasks represent development work still to be completed. With the exception of the first task, the X-band DRO development, these developments are not funded by the current research and development technology effort but are being pursued under other technology and flight hardware development programs.

(1) Complete the development of the X-band multi-channel DRO.

(2) Develop the Ka-band multi-channel DRO to cover Ka-band channels.

(3) Develop micro-miniature low-loss pre-select filters for S-band, X-band, and Ka-band receiver applications using high-Q dielectric resonator-based circuits.

(4) Develop micro-electro-mechanical (MEM) switches for X-band and Ka-band applications.

(5) Evaluate the S-band direct vector modulator for linear phase modulation, and BPSK/QPSK, and phased-array applications.

(6) Develop X-band and Ka-band vector modulators.

(7) Evaluate ferroelectric thin-film phase shifters and varactors. A novel phase-shifter technology developed under Defense Advanced Research Projects Agency (DARPA) utilizes ferroelectric thin-film technology to provide voltage-tunable X-band and Ka-band phase shifters with large linear tuning range. The tunable circuit products based on the ferroelectric barium strontium titanate (BST) are still under development and expected to be available within a year. We will continue to assess and evaluate these technologies and products for the advanced transponder and phased array and other space applications.

(8) Evaluate pseudomorphic high electron mobility transistor (P-HEMT) technology and heterojunction bipolar transistor (HBT) technology applicability for low-noise and high-power applications at X-band and Ka-band.

(9) Study the applicability of silicon–germanium (SiGe) RFIC technology to highly integrated, micro-miniature, low-power X-band transponder and ultra-high frequency (UHF) transceivers for Mars and other space applications. A four-chip architecture and solution will be attempted. The receiver, phase-locked-loop synthesizer, transmitter, and modulator functions will be included in the RF multi-chip configuration. Future spacecraft such as micro-satellites and Mars rovers for space exploration require micro-miniaturized communication systems with low power, low mass, and versatile communication systems. SiGe provides a high level of integration at low voltage and low power operation at low cost potential.

V. Digital Design Specifications and Analysis

A. Carrier-Tracking Loop Architecture

This section discusses the requirements and architectural trade-offs involved in the design of the carrier-tracking loop for the Advanced Transponder.

1. Key Requirements. The critical requirements driving the tracking loop architecture are as follows:

(1) Carrier threshold ≤ -155 dBm

(2) Deep-space Doppler tracking range $> \pm 200$ kHz

(3) Deep-space Doppler rate tracking > 400 Hz/s

(4) Doppler tracking range at S-band capable of supporting a lander–orbiter link for a worst-case MRO low orbit at Mars

(5) Doppler tracking rate at S-band capable of supporting a lander–orbiter link for a worst-case MRO low orbit at Mars

(6) Unconditionally stable loop or controlled instability for any input signal level from threshold to -70 dBm

2. Carrier Threshold. The carrier-lock threshold point can be defined (as for SDST and STM) as a carrier-signal-to-noise-power ratio of 0 dB. The lowest signal power, Pc_0, that satisfies this signal-to-noise ratio can then be given by the following expression:[6]

$$Pc_0 = k + T_0 + NF + 2B + SNR - L$$

where

$$k = \text{Boltzmann constant} = -198.6 \text{ dBm/K-Hz}$$
$$T_0 = \text{system temperature} = 293 \text{ K (room temperature)} = 24.7 \text{ dB-K}$$
$$NF = \text{receiver noise figure} = 2.5 \text{ dB (specified)}$$
$$2B = \text{two-sided loop tracking bandwidth at threshold, in dB-Hz}$$
$$SNR = \text{signal-to-noise ratio at threshold, defined as 0 dB}$$
$$L = \text{radio implementation loss } (-2 \text{ dB worst case})$$

So,

$$-155 \leq -198.6 + 24.7 + 2.5 + 2B + 0 + 2 = -169.4 + 2B$$

Or,

$$2B \leq 14.4 \text{ dB-Hz} = 27 \text{ Hz}$$

In other words, the loop should be designed with a two-sided bandwidth at a threshold of about 25 Hz.

This narrow loop bandwidth is necessarily at odds with the Doppler tracking performance, which gets better as the bandwidth increases. However, the low threshold is primarily driven by the X-band and Ka-band direct-to-Earth performance requirements, while the large Doppler tracking rate and range are primarily needed to support crosslink lander–orbiter links at S-band at signal levels significantly above

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[6] *Small Deep Space Transponder Group Buy Specification*, op cit., p. 39.

threshold. Here, we are aided by the automatic gain control (AGC) function preceding the carrier-tracking loop. The loop gain, and therefore the bandwidth, depends on the power level of the input signal. The AGC function serves to normalize the input signal level by the detected total power and therefore maintains a constant loop input power level, as long as the signal power is significantly greater than the noise power. As the signal power drops to the point where the noise contribution is significant, normalizing the input signal by the total detected power begins to reduce the actual signal strength and gain of the tracking loop. This in turn causes the bandwidth to contract for weak signals, which both enhances the detection threshold and reduces the tracking range. In the design of the STM AGC and tracking loop, a bandwidth compression factor of about 10 was obtained in going from strong signal to threshold. With a similar design, then, we expect to see a loop bandwidth of 200 to 250 Hz at strong signal.

3. Carrier Tracking. For standard second-order-loop damping in the range of 0.5 to 1, the natural frequency of the loop, ω_n, is roughly equal to the one-sided loop bandwidth. The Doppler tracking range of the loop then can be estimated by requiring that the acceleration error, $\Delta(d\omega/d\tau)/\omega_n^2$, be maintained reasonably small, or less than about 30 deg or so for reliable tracking [5]. For a ω_n of about 125 Hz then, we should be able to track a Doppler rate of about $(30/360) * 125 \text{ Hz}^2 = 1300 \text{ Hz/s}$.

The total Doppler tracking range can similarly be estimated by requiring that the residual tracking phase error be kept small. A second-order loop will track out a static frequency offset, but deviation from the ideal infinite-gain integrator will cause leakage resulting in a static phase error, given by the frequency offset divided by the loop gain: $2\pi\Delta f/K$. For total gain values of a few times 10^7, as achieved for STM, this results in a phase error of about 1 deg for an offset of 100 kHz. This implies that Doppler offsets of up to 1 MHz can be supported with a relatively small phase error. However, as the gain drops off at lower signal levels, this tracking range will shrink, and for signal levels about 10 dB above threshold and higher, we can expect to be able to track about ±500 kHz of static Doppler.

As seen from the requirements above, this performance is sufficient to meet the requirements for deep-space acquisition and tracking at X-band, but what about for proximity links at S-band?

As a way to bound the proximity Doppler requirements, we considered the worst-case low orbit of the planned Mars Reconnaissance Orbiter (MRO) (which will use a UHF proximity link). Trajectory simulator models for an MRO orbit at 200 km show[7] a peak Doppler rate of 90 Hz/s on a 400-MHz UHF carrier, and a total Doppler range during a pass of -5 kHz to $+5$ kHz. Since we plan to use S-band, at 2.1 GHz for proximity links with the Advanced Transponder, we need to scale these modeled numbers up by a factor of five to get proximity Doppler tracking rate and range requirements at S-band of 450 Hz/s for the rate and ±25 kHz for the range for a worst-case low-orbit pass.

The second-order loop parameters above would suggest that both the deep-space and proximity Doppler tracking rate and range requirements can be met with a second-order loop similar to that planned for STM. In addition, the second-order loop has the advantage of being simpler to analyze and, most importantly, of being unconditionally stable at all input signal levels and phases. For these reasons, we will implement the Advanced Transponder carrier-tracking loop as a second-order phase-locked loop.

In addition, because the tracking loop is closed digitally, we will be able to reprogram the tracking-loop filter parameters on the fly. This will allow us to expand the loop bandwidth and improve the tracking performance at the expense of signal threshold. For example, a factor of two expansion of the loop bandwidth will degrade the threshold by 3 dB, but provide a factor of four improvement in Doppler tracking rate. Since most proximity links will operate at strong signal levels, we can use this programmability to our advantage to optimize the tracking loop for the required application.

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[7] D. J. Bell, personal communication, MRO Telecom Systems Engineer, Jet Propulsion Laboratory, Pasadena, California, April 2003.

B. High-Rate Command Detector

In addition to the standard command detection unit (CDU), we also will provide a high-rate command detector (HRCD) in order to enhance the uplink command rate to 256 kb/s or more, compared to the SDST and STM maximum rates of 2 kb/s. The HRCD will demodulate PSK-modulated data from the uplink carrier. This section provides a description of the HRCD architecture and analysis.

The core of the HRCD is a straightforward integrate-and-dump detector with a digital phase-tracking loop. In the case of the transponder, we know that the bit rate is exactly synchronous with the master clock, since the master clock is adjusted to track the received carrier. This simplifies the design problem, as we have only one variable to track, the bit timing, as opposed to the traditional PLL bit detector where both frequency and phase must be recovered and tracked.

Bit synchronization is acquired and maintained by using the early/late gate-type tracker. In this approach, three parallel integrate-and-dump detectors are used, with the relative phases staggered. The loop attempts to keep the value of the center detector maximized relative to the others, deriving the error signal from the difference of the differences. A timing diagram is provided in Fig. 15.
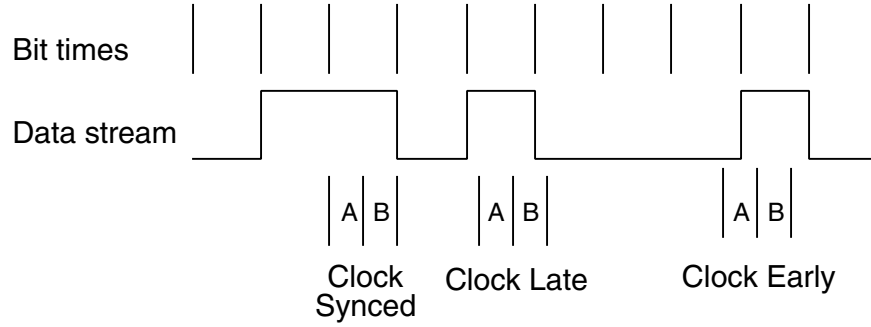
Fig. 15. HRCD bit timing diagram.

The average output of the early (or late) filter is

$$\text{output} = \bigl(1 - \text{abs}(\text{relative timing error})\bigr)$$

This results from the average value of the preceding or following bit being zero (assuming that bits are $+1$ or -1).

The "error" signal used to drive the tracking is formed by calculating (averaging is over many bit times):

$$\text{early difference} = \text{average}\bigl(\text{abs}(\text{center filter})\bigr) - \text{average}\bigl(\text{abs}(\text{early filter})\bigr)$$

$$\text{late difference} = \text{average}\bigl(\text{abs}(\text{center filter})\bigr) - \text{average}\bigl(\text{abs}(\text{late filter})\bigr)$$

$$\text{control signal} = \text{early difference} - \text{late difference}$$

where control signal > 0 indicates that the dump timing is late, and the converse if the control signal is negative.

In a practical implementation of this approach, the integration is done in two stages. First, the input samples are accumulated in a high-rate integrate and dump, with samples "dumped" at a convenient rate, typically 16 or 32 times the bit rate. The $16\times$ bit-rate samples then are summed to produce the final output. Design trade-offs can be made to select the precision and number of stages for each integrate and dump to optimize power dissipation (the lower-frequency stages clock at slower rates and consume less power). A block diagram of the HRCD is shown in Fig. 16.

In our implementation, the outputs of the three detectors (after averaging) are compared and used to determine whether to add or drop a clock pulse from the counter that determines the timing of the integrators. This moves the filter timing one step later or earlier.

The tracking-loop performance is a combination of the amount of early/late timing stagger, the length of time over which the filter outputs are averaged, the frequency of clock adjustments, and the size of the clock step. The highly non-linear nature of the entire tracking and detection process makes simulation the preferred means to evaluate changes in the design parameters. Sample bit streams can be created with varying noise and bandwidth characteristics and processed through the tracking algorithm, with actual bit-error rate (BER) measurements made.

A program has been created to perform these simulations with all the calculations performed in double precision floating point (so that we can explicitly control the round off and quantization effects). A random bit stream is generated and sampled at the specified rate. Additive white Gaussian noise is added with a suitable random number generator, with the variance adjusted to reflect the appropriate SNR. The noisy signal then is passed through a simple digital filter to represent the analog filtering prior to digitization. Currently, filters with Butterworth shapes are being used, but standard filter synthesis programs (e.g., Matlab) can generate coefficients for any desired filter characteristic. The filtered signal is quantized with a model of a saturating ADC. In the current simulation, a perfect ADC is assumed (ideal quantization, no jitter, no differential non-linearity); however, it is a straightforward matter to assess the effects of non-ideal quantizers.

The integrate and dump filters and the tracking logic are implemented algorithmically using the integer outputs of the quantization process. For analysis purposes, we can simulate the output of a large number of parallel integrate-and-dump filters, each at a different relative timing. The plots of the output of this process, while resembling familiar "eye diagrams," are really a graphical representation of the probability distribution function of the filter outputs. Figure 17 shows the results of a simulation using ideal integrate-and-dump filters.

VI. Phase Noise Analysis

A critical parameter of the receiver tracking and downlink synthesis loop performance is the phase noise. This section presents a preliminary analysis of the X-band front-end transponder architecture. The design presented will allow for in-flight tuning of the receive frequency to cover the entire 50-MHz DSN band. A discussion of the phase noise is presented, and a number of issues requiring further investigation are listed. Later, in Section VII, measurements of the phase noise using a prototype DRO-PLL are presented.

A. Front-End Operation

A block diagram of the nominal X-band front end was given in Fig. 16. The RF uplink is at a frequency of 7149 to 7190 MHz with an information bandwidth of about 5 MHz (keeping the first couple harmonics of the ranging tone). The uplink frequency is defined as $749 * fo + fk$, where fo is about 9.45 MHz and fk ranges from 70 MHz to 110 MHz, as tabulated for a few DSN channels in the figure.

After amplification in an LNA, the uplink is downconverted to $13 * fo$, scaled in an analog AGC, and digitized at $4 * fo$ to present quadrature samples to the digital processor.
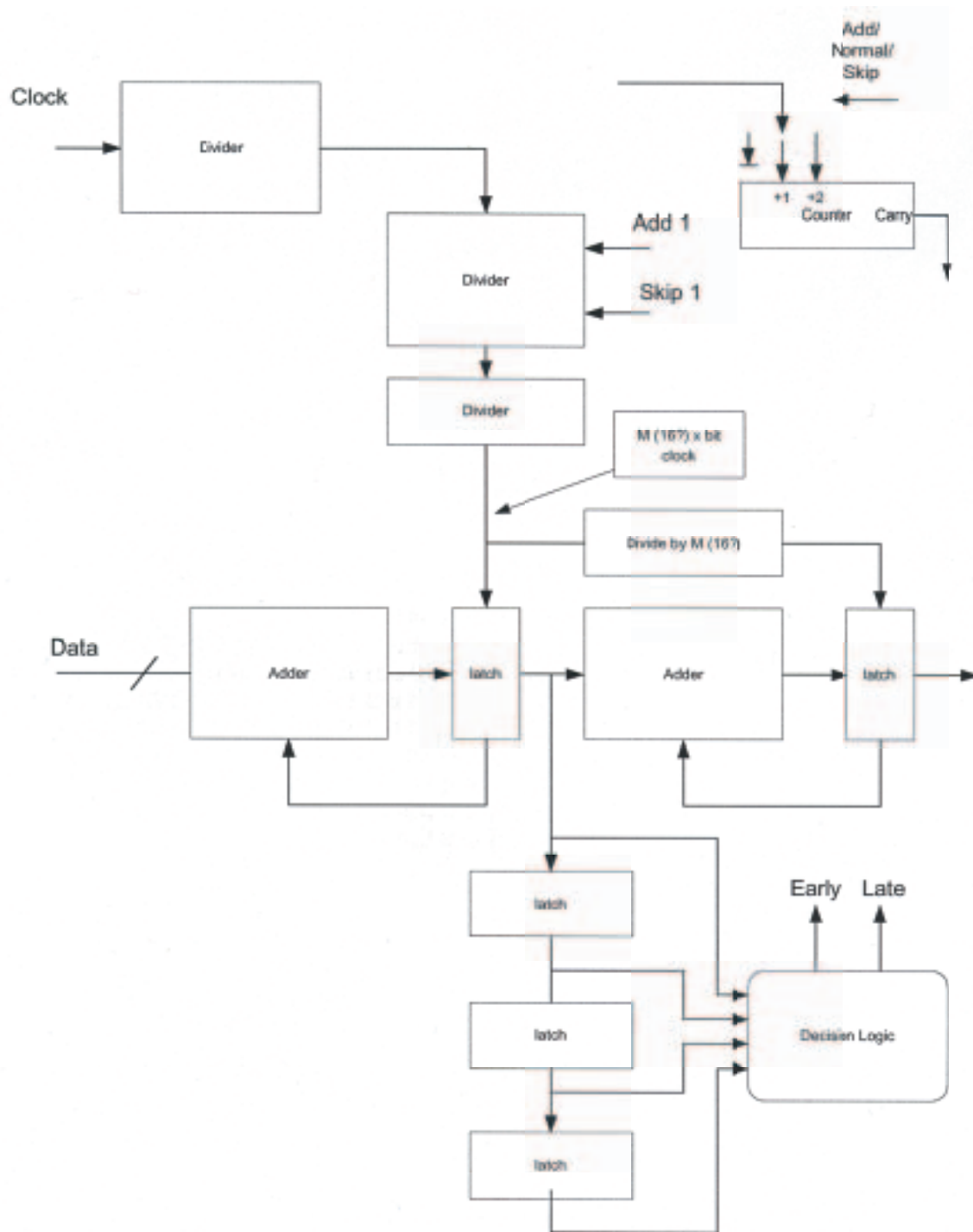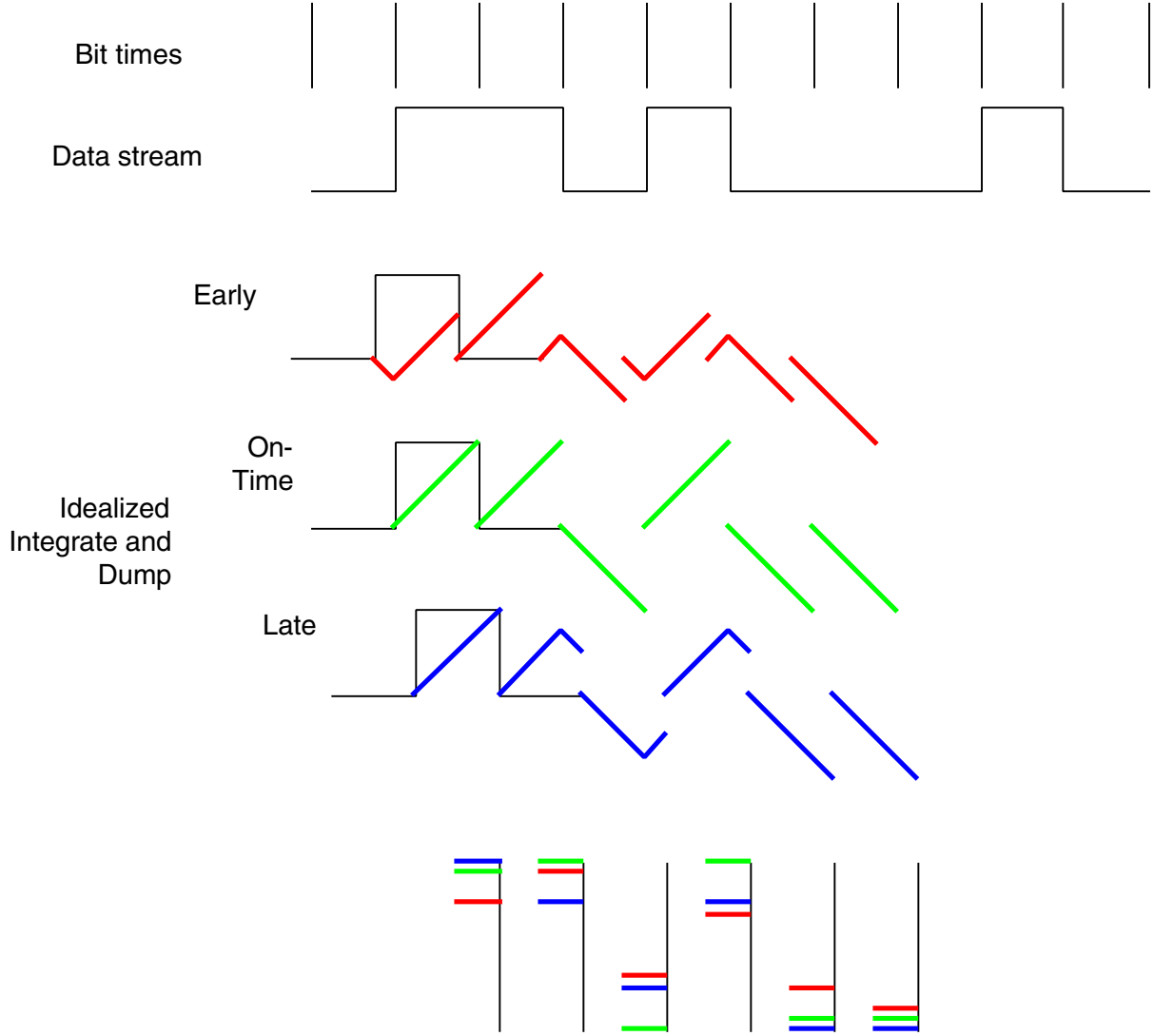
Fig. 16. HRCD block diagram.

Fig. 17. Ideal integrate-and-dump operation of HRCD.

The downconversion is accomplished using a DRO-PLL. The DRO operates at a frequency of $736 * fo + fk$ and is tunable over the 50-MHz range of fk by applying a DC bias derived from a bias DAC that is digitally programmable. The ability to pull the DRO frequency over this range was demonstrated in the laboratory; see Section VII. Using a new DRO design, we were able to increase the DRO tuning range from the $\sim$10-MHz STM design to >50 MHz. The DRO output is mixed down to DC using a sampling phase detector (SPD). The SPD step-recovery diode is driven by the upper sideband produced by mixing the reference oscillator ($\sim$151 MHz) and a digitally synthesized $fk/46$ sine wave ($\sim$1.5 to 2.5 MHz). Note that the bandpass filter after this mixer must pass the upper sideband ($\sim$151.5 to 152.5 MHz) but reject the lower sideband ($\sim$149.5 to 148.5 MHz). A selection criterion for the fo and fk combination will be the ease of constructing this filter; larger values of fk will simplify the filter and increase the spacing of leak-through harmonics in the PLL but will also reduce the oversampling factor of the receiver NCO/DAC and degrade the phase noise. Work done in the laboratory suggests that about 10 MHz may be a better choice for fk.

The sampling phase detector will sample the DRO with the 46th harmonic of the (oscillator) $\times$ (receiver NCO) signal, producing a phase-error signal that will be filtered and combined with the overall

DC bias voltage to control the DRO frequency. This error signal will be applied to the lightly coupled varactor port of the DRO. The tightly coupled port will be used for quasi-static channel-selection tuning using a bias DAC. An issue that must be investigated is how much noise pickup can be tolerated on the bias DAC output. By design, the DRO frequency will be very sensitive to voltage variations on this signal, and any noise will cause frequency modulation that will appear on the $13fo$ IF carrier. However, the bias DAC signal can be filtered with a very long time constant if necessary, as there is no operational requirement to rapidly switch DSN frequency.

1. Loop Phase Noise. Phase noise on the DRO will appear on the $13fo$ IF and degrade the navigation and communications performance of the transponder.

The main architectural difference between this design and that used in STM is that here the reference oscillator is mixed with the receiver NCO frequency before "multiplication" in the sampling phase detector. In the STM design,[8] the reference oscillator is used to sample the DRO, and the resulting IF (around 8 MHz) then is mixed with the receiver NCO output. If the phase noise of the NCO is larger than that of the reference oscillator, then the current design clearly will be limited by the NCO since its phase noise will be multiplied up in the SPD. Theoretically, however, the phase noise of the NCO output should be lower than that of the reference oscillator by $20 * \log(2 \text{ MHz}/150 \text{ MHz})$, or -43.5 dB, since the NCO is referenced to the reference oscillator. However, the DAC itself contributes a certain noise floor due to random thermal effects, etc., which prevents the lower bound from actually being reached. So, the requirement for this design is that the intrinsic noise floor of the DAC (and to some extent the upstream electronics) not exceed the phase noise due to the reference oscillator. If this condition is met, this architecture actually will produce an improvement of 6 dB over the STM design since the reference is multiplied by 46 instead of 92 due to the reference frequency going from $8 * fo$ to $16 * fo$. (Of course, the 152-MHz oscillator may have 6-dB worse phase noise performance than the 76-MHz oscillator if they both are derived by multiplication of a lower-frequency crystal reference).

To look at some sample numbers, a very good low-noise crystal oscillator in the 100-MHz range may have a phase noise performance of around -155 dBc/Hz at 1 kHz, flattening to -160 dBc/Hz at 10 kHz [6] (although note that the Deep Space Transponder (DST) specification sets the input phase noise of the ultra-stable oscillator (USO) at only -125 dBc/Hz at 10 kHz—significantly worse performance). As this reference is multiplied up in the SPD by a factor of 46, the phase noise will degrade to about $-160 + 20 * \log(46) = -126$ dBc/Hz at 10 kHz.

Theoretically, phase noise of the NCO output would be improved by -43 dB over the reference oscillator it is locked to, or about -200 dBc/Hz. However, the noise floor of the DAC component will limit this improvement. Noise floors typically are better than -165 dBc/Hz for transistor–transistor logic (TTL) parts, to -150 dBc/Hz for emitter-coupled logic (ECL) parts, and some PLL ICs have noise floors as high as -130 dBc/Hz.[9] For parts at -165 dBc/Hz, the NCO noise will not significantly degrade the reference oscillator noise, and the reference oscillator will dominate the loop performance. For an ECL-type part at -150 dBc/Hz, the NCO will be the dominant contribution, and the overall phase noise of the loop, after the factor 46 multiplication, will be about -110 dBc/Hz at 10 kHz. By contrast, the STM architecture would hide the noise floor performance of this part because it would enter the loop after the $\times 92$ multiplication, and the overall loop would run at -126 dBc/Hz for the oscillator performance given above.

What sort of performance do we need? The most relevant specification is the phase noise performance required of the downlink carrier, operating in coherent mode. In this mode, the phase noise will be due to the combination of the uplink DRO loop phase noise entering the IF and the downlink DRO loop phase

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[8] S. Kayalar, "STM 736 fo DRO PLL Design," JPL Interoffice Memorandum 3366-00-015 (internal document), Jet Propulsion Laboratory, Pasadena, California, May 5, 2000.

[9] EMF Systems, Inc., State College, Pennsylvania.

noise (which will be nearly identical in design). The Deep Space Transponder specifies that the phase noise power spectral density on the downlink in this mode be below −93 dBc/Hz at a 10-kHz offset from the carrier and below −125 dBc/Hz at a 25-MHz offset from the carrier. Assuming that the receiver and synthesizer DRO loops contribute equally, we would conclude that the performance should be better than about −96 dBc/Hz at 10 kHz. This would suggest that even with some noise-floor degradation due to the DAC, we can still meet this requirement. Note that the wideband performance requirement of −125 dBc/Hz at 25 MHz will really be placed on the DRO. This is beyond the PLL loop bandwidth and, therefore, will not be affected by the loop architecture. A typical X-band DRO should be able to achieve around −140 dBc/Hz or better at deviations beyond 1 MHz.

2. Open Issues. There remain a number of open issues to be worked. Some are listed below:

(1) The DRO frequency tuning range must be investigated—preliminary laboratory work has demonstrated a >50-MHz tuning range.

(2) Noise power levels on the bias DAC must be investigated and a maximum FM noise on the DRO specified.

(3) The choice of fo and fk should be optimized.

(4) The noise floor of the DAC and associated components must be investigated in more detail. Preliminary laboratory work with the NCO shows promise, but spurious noise in the 100-kHz range due to internal FPGA switching noise currently is limiting the measurements. Follow-on work employing Schmidt-trigger buffers should mitigate this problem.

VII. Experimental Results

In order to establish the feasibility of our architecture, we developed breadboard hardware in the laboratory using residual hardware from the STM development when available and designing new components when required.

A. X-Band DRO with Dual Varactors

A key aspect of the Advanced Transponder architecture is the ability to tune the frequency of the receiver and transmitter dielectric resonance oscillators (DROs) in order to cover the entire DSN band. To demonstrate this principle, we designed and fabricated a dual-varactor DRO substrate and populated it with a voltage-controlled oscillator (VCO) MMIC, two varactor diodes, and a dielectric puck from STM residual stock. Figure 18 is a photograph of one of the X-band DROs we fabricated for this effort.

In this DRO design, the loosely coupled varactor, pictured above the dielectric puck in Fig. 18, is used for fine tuning of the DRO frequency and is the control port used to close the phase-locked loop. The tightly coupled varactor is shown to the left of the puck and is designed to be driven by the output of a coarse frequency control, or channel-select digital-to-analog converter (DAC). This DAC output is heavily low-pass filtered and is designed to hold a quasi-static tuning voltage for DSN frequency channel selection. The DROs designed for the STM development were designed to have a tuning range of about 10 MHz. For this development, we went to two varactors in order to achieve a tuning range greater than the DSN allocation bandwidth of 50 MHz at X-band in order to provide in-flight channel selection. Laboratory measurements of our prototype design have demonstrated that tuning ranges of greater than 60 MHz are possible, as shown in Fig. 19.

In order to demonstrate the operation of the DRO in the relevant phase-locked loop environment, we used an Alpha sampling phase detector from STM residual stock to put together a simple first-order loop to phase lock the DRO to a frequency reference provided by an HP 8663 synthesized frequency generator. A block diagram of the laboratory setup is shown in Fig. 20.
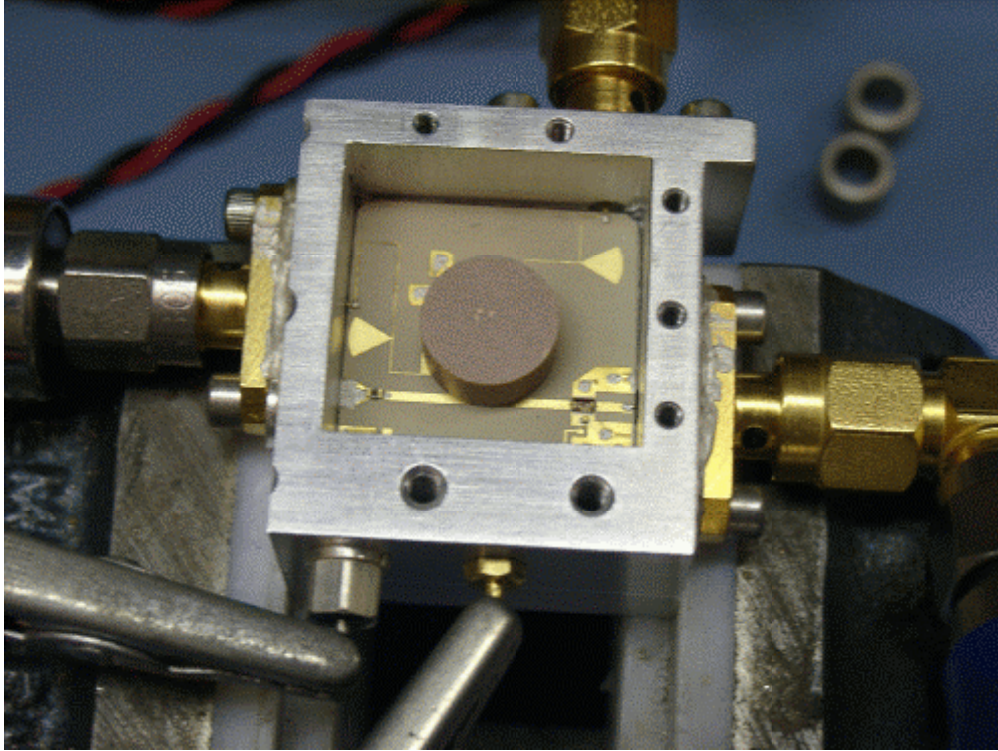
Fig. 18. X-band DRO fabricated for the Advanced Transponder. The design uses a negative resistance VCO to excite the DRO oscillations and two variable capacitance varactor diodes for frequency tuning. The varactor trace to the left of the puck is tightly coupled for coarse tuning, and the one above the puck is more loosely coupled for fine tuning. The circuit board pictured is approximately 20 mm $\times$ 20 mm.
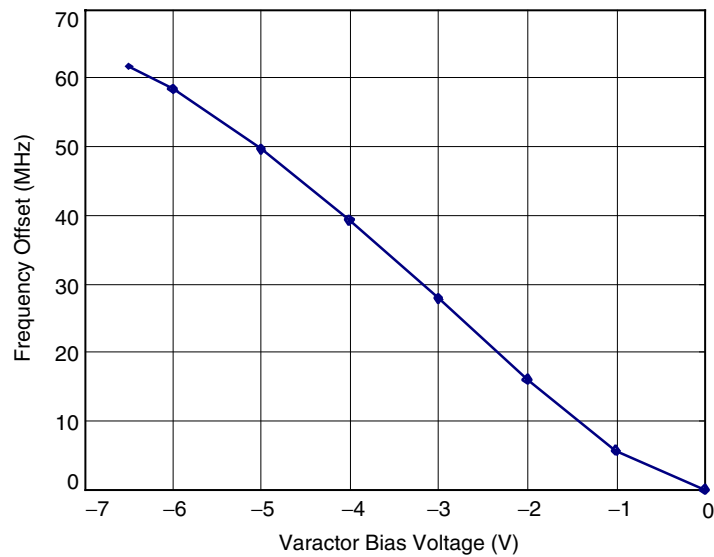

Fig. 19. DRO frequency offset in MHz versus applied varactor bias voltage, using tightly coupled varactor layout. A tuning range of >60 MHz is demonstrated for a bias voltage range of 0 to −6.5 V.

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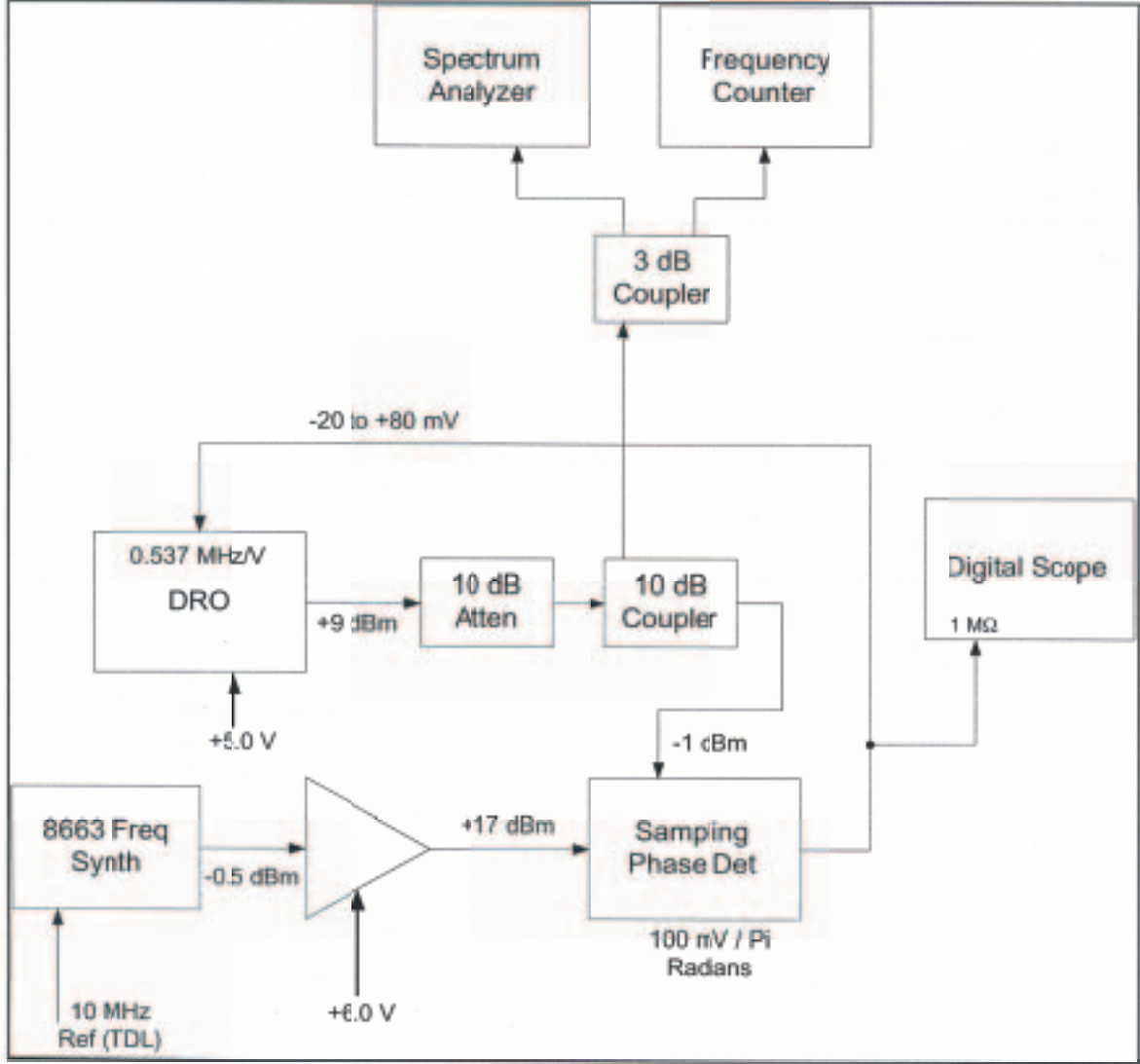
Fig. 20. Laboratory setup to demonstrate phase locking of X-band DRO to 160-MHz frequency reference.

The sensitivity of the DRO tuning port was measured to be -0.54 MHz/V for small signal variations, and the SPD sensitivity was measured by driving the SPD with the 160-MHz signal from the HP 8663 and an X-band signal generated by an HP 83731A. By slightly detuning the frequencies, we generated a low-frequency beat note at the output of the SPD and used it to measure the slope as about 100 mV/cycle. Figure 21 shows a simplified loop diagram of the setup from which we can write down the basic loop equation:

$$\theta_0(s) = \big(\theta_i(s) - \theta_0(s)\big) Kp\, Kv/s$$

$$\theta_0/\theta_i = [Kp\, Kv]/[s + Kp\, Kv]$$

and

$$\theta_e = \theta_i[s\, Kp]/[s + Kp\, Kv]$$
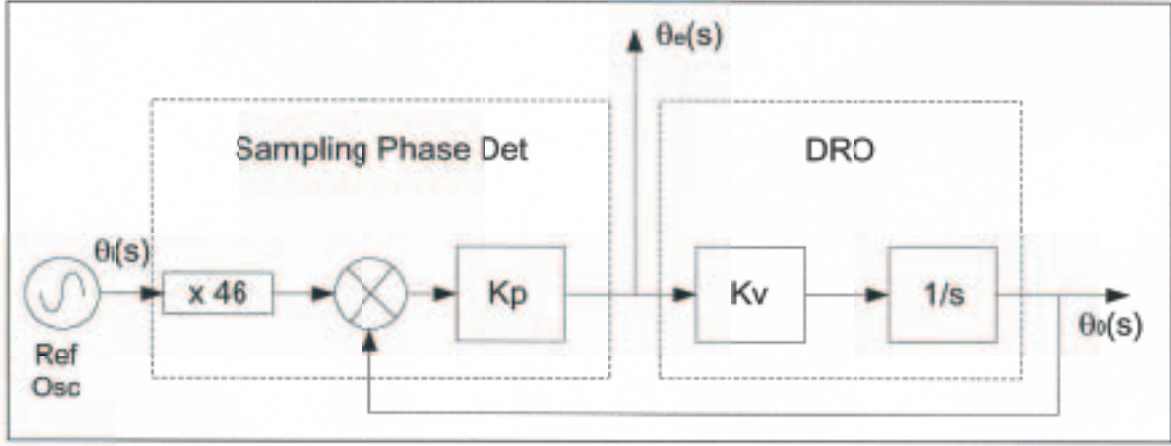
Fig. 21. Diagram of experimental first-order phase-locked loop setup.

where the symbols are defined as follows:

$$\theta_0(s) = \text{DRO output phase}$$

$$\theta_i(s) = \text{reference oscillator phase}$$

$$kp = \text{phase detector gain}$$

$$kv = \text{DRO gain}$$

$$s = \text{the Laplace variable}$$

$$\theta_e(s) = \text{phase error}$$

$$Cv = \text{magnitude of frequency step}$$

Now if we apply a frequency step at the input to the SPD, we get the following response:

$$\theta_i = Cv/s^2$$

$$\theta_e = Cv[s\,Kp]/s^2[s + Kp\,Kv]$$

Then taking the inverse Laplace transform to get back to the time domain, we get

$$\theta_e(t) = e^0[Cv\,Kp]/[Kp\,Kv] + e^{-Kp\,Kv\,t}/[-KpKv]$$

$$\theta_e(t) = Cv/Kv - e^{-Kp\,Kv\,t}/[KpKv]$$

So, as $t \rightarrow INF, \theta_e(t) \rightarrow Cv/Kv$.

Experimentally, we applied a frequency step by jumping the frequency of the 8663 synthesizer by -100 Hz. On the digital scope, we observed a jump of $+9$ mV in the error voltage feeding back into the DRO. Because we designed the loop to lock the DRO frequency to the 46th harmonic of the HP 8663 frequency reference, a -100-Hz step in the reference frequency is equivalent to a -4600-Hz step in the DRO frequency for the locked condition, so $Cv = -4600$ Hz in the above expression for the frequency step. The DRO gain, Kv, was measured to be -0.54 MHz/V, so $Cv/Kv = -4600$ Hz$/-0.54$ MHz/V $=$

8.5 mV error step. This calculated value agrees well with our measured 9 mV, showing that our DRO-PLL loop is quantitatively well understood.

We also attempted to quantitatively understand the settling time constant of the error voltage. Experimentally, the error voltage step initially overshot to about 12 mV, and then settled down to 9 mV after about 200 μs. From the equations developed above, the time-dependent response should be described by the following exponential:

$$\theta_e(t) = Cv/Kv - e^{-Kp\,Kv\,t}/[KpKv]$$

The curve given by this expression will exponentially approach the 9-mV level from below and should not overshoot. Also, the measured values of 0.54 MHz/V for the DRO sensitivity and 100 mV/cycle for the SPD gain suggest a time constant of $Kp\,Kv = 54,000$/s, or $1/(Kp\,Kv) = 18$ μs, so response looks much slower and has the wrong shape. Most likely, we are seeing the frequency response of the HP 8663 recovering from the programmed 100-Hz jump. The HP 8663 has a frequency sweep feature, but the fastest update rate it is designed for is 0.5 ms, so its own internal PLL is designed with a time constant of 100 μs or so, which is what is observed on the DRO voltage control line. The frequency response of our DRO-PLL is much faster and actually tracks the settling of the HP 8663 frequency synthesizer.

We also experimentally determined the tracking range of the DRO-PLL loop with this simple first-order filter. We locked the DRO-PLL and adjusted the reference oscillator frequency in steps of 10 Hz. The loop tracks through a reference oscillator frequency range from 161.619850 MHz to 161.618570 MHz, or a range of 1280 Hz. This corresponds to $1280 * 46 = 58,880$ kHz at the DRO. This range also corresponds to -20 mV to $+80$ mV on the DRO control voltage line. This means that the SPD is essentially operating to the rails. The 3-dB bandwidth of a first-order loop is equal to K, the total loop gain. From the calculation of $Kp\,Kv$ given previously, the 3-dB loop bandwidth is 54 kHz. The hold-in range of the loop is given by a condition on the phase error of the loop: phase error $= \Delta f/K$, where Δf is the frequency offset. And, in fact, if we don't make the linear small angle approximation, sin(phase error) $= \Delta f/K$. This says that $\Delta f/K$ has to be less than 1 or the loop can't remain in lock. So, theoretically, this loop should have a hold-in range of about 54 kHz, and experimentally, we demonstrated that it will track 58.8 kHz. Again, the close agreement suggests that our simple DRO-PLL loop is behaving as expected.

B. Digital Results

One of the challenging aspects of the digital design of this transponder architecture is the high speed and high resolution of the receiver and synthesizer numerically controlled oscillators (NCOs). In order to demonstrate the feasibility of the NCO and high-speed sine look-up table, we purchased a Xilinx Virtex II field programmable gate array (FPGA) and a development board to use as a digital prototyping platform. Figure 22 is a photograph of the development platform set up in the laboratory.

The stringent requirements on the NCO performance come from the sensitivity of the Block V receivers in the Deep Space Network. Although most missions request that the Block V receiver be configured for a tracking-loop bandwidth of 10 Hz to 3 Hz, some radio science missions could ask for bandwidth settings as low as 1 Hz or even 0.1 Hz. If we take 0.1 Hz as our most stringent requirement, we need to make sure that in frequency slewing to track Doppler, the size of our minimum frequency step is small enough that the Block V receiver does not drop lock. In order to ensure this, we need the step size to be at least a factor of 10 smaller than the minimum Block V loop bandwidth, or less than 0.01 Hz. Furthermore, since the NCO frequency reference is multiplied up in the sampling phase detector (SPD) in the downlink module, the frequency resolution of the NCO itself must be correspondingly better. The worst-case multiplication factor is 209 for Ka-band downlink synthesis. Therefore, to meet the 0.01-Hz resolution at Ka-band, the frequency resolution of the NCO must be 0.01 Hz/209 = 0.00005 Hz, or 0.05 mHz. Furthermore, the NCO must operate at a very high clock rate of 160 MHz, so in order to meet
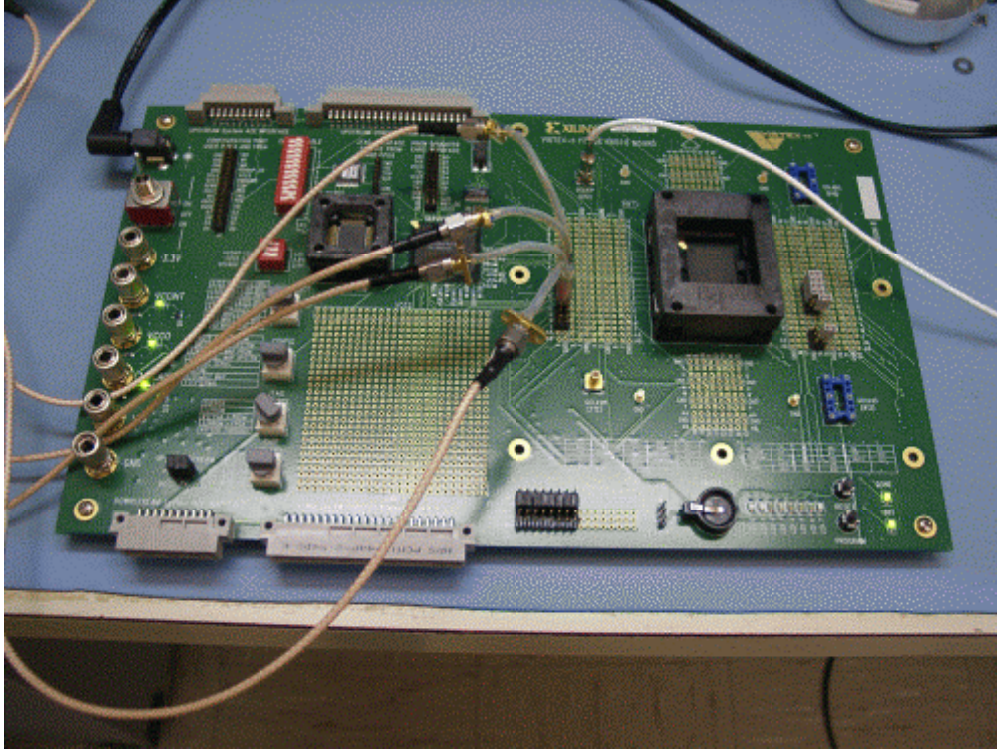
Fig. 22. Xilinx Virtex II development board setup in the laboratory and configured as a high-speed NCO.

this specification, the size of the NCO must be $2^N = 160$ MHz/0.05 mHz, or $N = 42$ bits. This then requires that the digital architecture must support a 42-bit full adder operating at 160 MHz.

To evaluate the feasibility of this NCO design, we designed an NCO with a 42-bit phase accumulator and 38-bit frequency word to support frequency programmability from 0 to 10 MHz. We developed the NCO design and test benches in the Verilog hardware description language and used the Cadence Verilog-XL tools for simulation and verification. The design was synthesized using the Xilinx design libraries and the Synplicity Synplify synthesis tool. The physical design was performed using the Xilinx Alliance Map and Place & Route tool, and the design was uploaded to the Virtex prototype board using a serial programmer and the Joint Test Action Group (JTAG) boundary scan port to program the electrically erasable programmable read-only memory (EEPROM) chip.

To translate the NCO phase word to a sine-wave amplitude, we used a sine look-up table (LUT) implemented as a read-only memory (ROM) addressed at each 160-MHz clock edge by the 10 most-significant bits of the current phase word. In order to conserve memory size, we store only one quadrant of the sine wave (0 to 90 deg) and use the two most-significant bits of the phase word to identify the quadrant and the other 8 bits to address the look-up table memory. Each amplitude word stored in the memory is 13 bits wide, for a total storage requirement of 13 bits $* 2^8$ addresses $= 3.24$ kbits. The 13-bit unsigned output of the sine LUT then is increased to 14 bits by the addition of a sign bit and conversion to 2's complement determined by the phase quadrant. The amplitude word then is rounded to 8 bits and output off the chip to drive a digital-to-analog converter (DAC) for sine-wave synthesis. In the future, the simple rounding may be modified to include amplitude dithering in order to reduce spurious content at the DAC output.

To test the NCO/sine LUT, a simple interface was designed to allow a fixed set of frequencies to be selected using a set of four jumpers placed on a header soldered to the development board. The

fixed frequencies were carefully selected to pick some frequency words that would ensure full exercise of the 42-bit accumulator carry chain and others that were harmonically related to the clock frequency and therefore would be expected to work at much higher clock frequencies. The NCO was exercised using an HP 8663 to generate the 160-MHz clock frequency. At 160 MHz, all programmed frequencies were observed to operate correctly. The clock frequency then was increased to determine the maximum operating frequency. The timing analyses performed by the synthesis and Place & Route tools reported the maximum predicted frequency of operation to be 180 MHz, but this estimate takes into account worst-case temperature and voltage margins. At the nominal 1.5-V core and 3.3-V input/output (I/O) voltage and at ambient temperature, we were able to increase the clock frequency to nearly 280 MHz before seeing evidence of timing errors affecting the NCO operation. Figure 23 is a photograph of the Xilinx prototype board in operation with the 4 most-significant bits of the sine LUT output displayed on a digital scope.

The original design of the DRO-PLL loop (shown in Figs. 2 through 13) uses the NCO to index a sine look-up table, the output of which drives a DAC for direct digital synthesis of the ∼10-MHz variable reference. This variable reference then is mixed with the fixed 160-MHz reference oscillator, and the upper sideband is filtered and used to drive the SPD. However, we came up with a novel approach to this architecture that may allow a drastic simplification of this circuit, eliminating the sine look-up table, the DAC, and the reference oscillator mixer. Figure 24 shows a comparison of the architectures we are now investigating. The first is the original design using a sine look-up table and DAC. The second eliminates the sine LUT and the DAC by driving the reference mixer directly with the square-wave most-significant bit (MSB) output of the NCO. This approach potentially eliminates analog switching and spurious DAC noise in the PLL as well as simplifying the architecture by eliminating discrete parts. The third architecture takes this a step further by also pulling the reference mixer into the digital processor and generating the sampling phase detector reference digitally. Here, the MSB of the NCO is XOR'd (multiplied) with
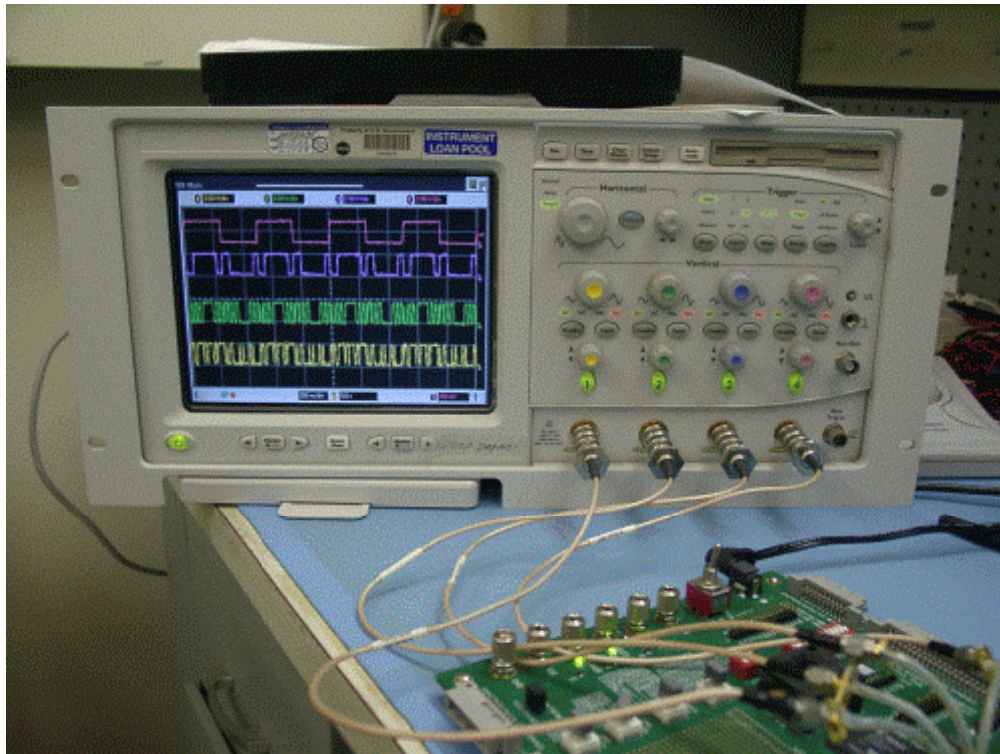

Fig. 23. Xilinx Virtex II prototype board generating synthesizing sine-wave downlink using 42-bit NCO and sine look-up table.
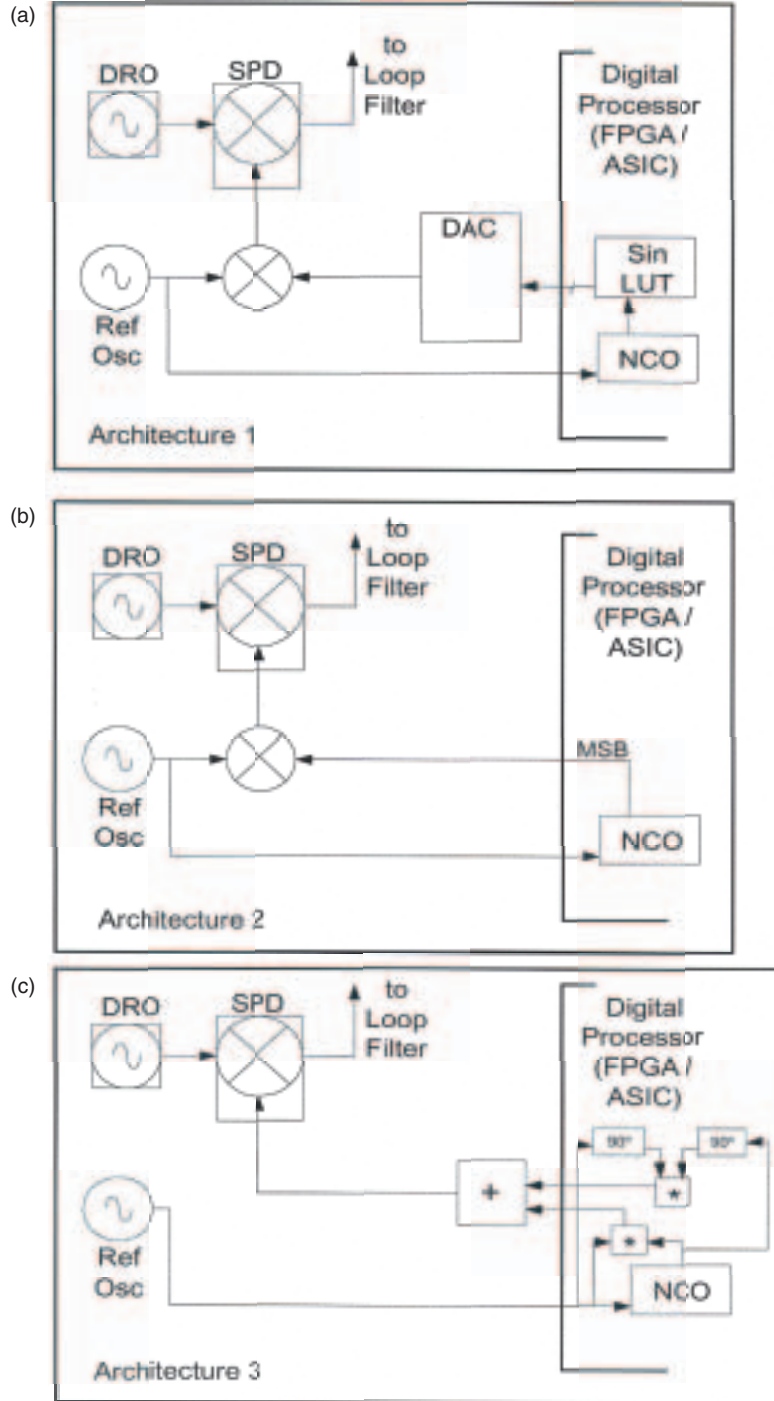
Fig. 24. Architectures for the NCO interface to the DRO-PLL: (a) Architecture 1 uses a sine look-up table and DAC to drive the reference mixer, (b) Architecture 2 eliminates the sine look-up table and DAC by driving the reference mixer directly with the NCO MSB, and (c) Architecture 3 pulls the reference mixer inside the digital processor by using a digital mixer. This third architecture also implements a digital single-sideband mixer to cancel the unwanted lower sideband mixing product and thereby relaxing the requirements on the analog filter (not shown) preceeding the sampling phase detector.

the synchronized clock, digitally generating the upper and lower sideband mixing products, nominally at 160 MHz and 140 MHz for a 150-MHz clock and 10-MHz NCO programmed frequency. In order to relax the requirements on the analog filter that is required to remove the lower sideband before driving the SPD, we implemented a single-sideband mixer inside the FPGA using a delay-locked loop to generate a 90-deg-delayed clock signal, and logically generating a 90-deg-delayed NCO MSB signal. The two signals then are analog summed outside the FPGA to cancel the out-of-phase lower sideband.

Architecture 3, depicted in Fig. 24(c), was implemented in the Xilinx Virtex II FPGA prototype board. By analog summing the two phases of the single-sideband mixer in a 17-ohm combiner, we were able to demonstrate a 20-dB suppression of the lower sideband with respect to the upper sideband, and a suppression of the clock-frequency "carrier" by 35 dB. However, in our breadboard setup, we used the low-voltage complementary metal oxide semiconductor (CMOS) output of the FPGA directly. These signals are not optimized for waveform shape since they are intended simply to provide digital levels. We expect to see marked improvement in the lower sideband cancellation and a much cleaner waveform by following the FPGA CMOS outputs with some high-speed Schmidt-trigger buffers to square up the signal before the analog combining.

To demonstrate the feasibility of this architecture, we used this digital single sideband (DSSB) mixer to drive the sampling phase detector, and we were able to achieve phase lock on the DRO using this method. However, digital switching noise and waveform irregularities produced significant close-in phase noise, and we have not yet been able to demonstrate that this technique can be used practically for the low-phase-noise performance we require. However, future improvements to the breadboard, including the Schmidt-trigger buffers mentioned above, should significantly improve the performance.

C. Phase Noise Measurements

An important performance parameter of the RF front-end and digital tracking architecture is the phase noise of the synthesized downlink and uplink tracking loop. We put together a phase noise measurement system in the laboratory in order to investigate this parameter for our breadboard DRO and associated circuitry. Figure 25 is a block diagram of the phase noise test setup.
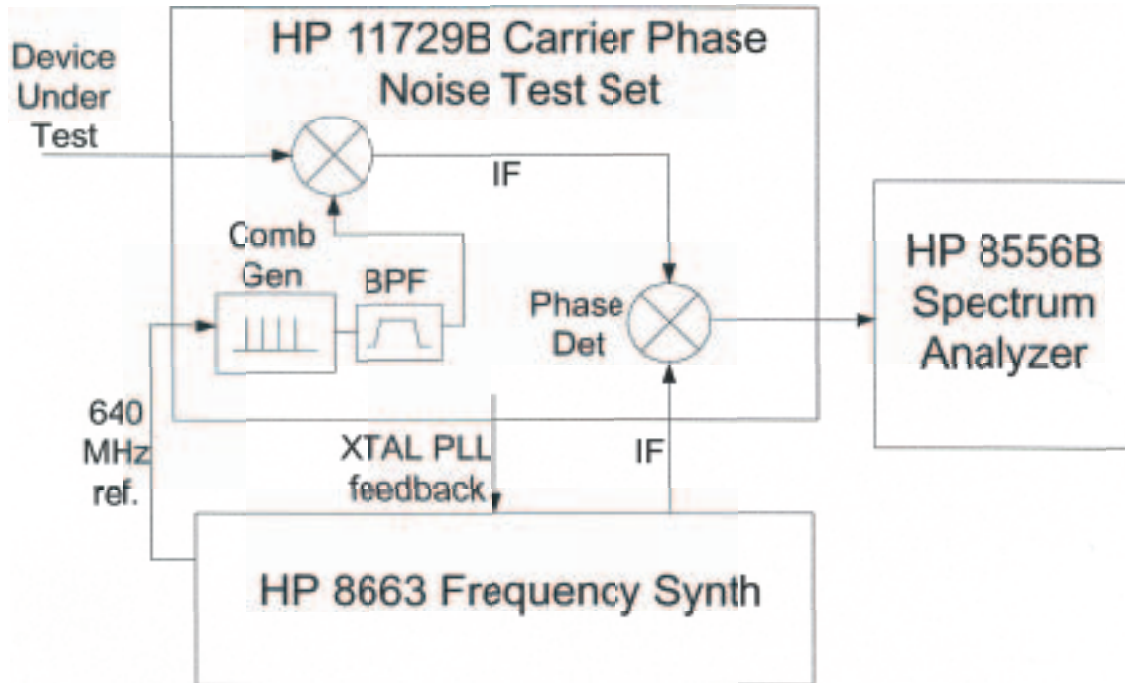

Fig. 25. Laboratory phase noise measurement system setup.

The device under test (DUT), the DRO in this case, is mixed with a harmonic of the precision 640-MHz reference from the HP 8663 frequency synthesizer. The IF then is beat against a reference IF generated by the HP 8663, and the baseband phase deviations are measured using an HP 8556B Spectrum Analyzer, which is sensitive down to 100 Hz. In practice, we found that measuring phase noise with this setup at frequency deviations of less than about 500 Hz was difficult due to interactions with the narrowband phase-locked loop that keeps the DUT signal and the reference IF signal in quadrature by frequency modulating the internal 10-MHz crystal oscillator in the HP 8663.

In our DRO-PLL setup (see Fig. 21), the sampling phase detector actually uses the 46th harmonic of the 153-MHz reference oscillator to beat against the DRO frequency of 7.038 GHz. The 46th harmonic will necessarily exhibit an increase in phase noise over the reference itself by a factor of $20*\log(46) = 33.2$ dB. Figure 26 shows the measured phase noise performance, using the setup described above, of the 153-MHz reference oscillator and the calculated increase due to the multiplication by 46. Also shown is the phase noise performance of the free-running unlocked DRO. However, because of the close-in instability of the free-running DRO, the tracking-loop bandwidth of the HP 11729 is insufficient to keep the DUT and the IF frequency in quadrature, and this measurement cannot be performed with the phase noise setup described above. Instead, the spectral noise density of the DRO was measured directly at 7 GHz using a spectrum analyzer. This method introduces some systematic errors in that the noise floor of the spectrum analyzer itself is significant, and the direct spectral density measurement is sensitive to both amplitude and phase noise. So, the phase noise spectral density of the free-running DRO is likely overestimated by this method, and we will need to work on improving this measurement.

From Fig. 26, it is clear that the close-in performance of the DRO is much worse than the ×46 reference oscillator, but that at large frequency offsets, the DRO performance beats the reference oscillator. The ideal design point for the DRO-PLL loop bandwidth is near the point at which the two curves cross; the performance inside the loop bandwidth will be determined by the reference oscillator, and outside the loop, the DRO will free run. Figure 27 is a plot of the measured phase noise of the DRO once the PLL has been locked. Indeed, the shape of the phase noise curve shows that the performance follows the reference oscillator inside the loop bandwidth of about 50 kHz, and that it follows the free-run DRO curve outside
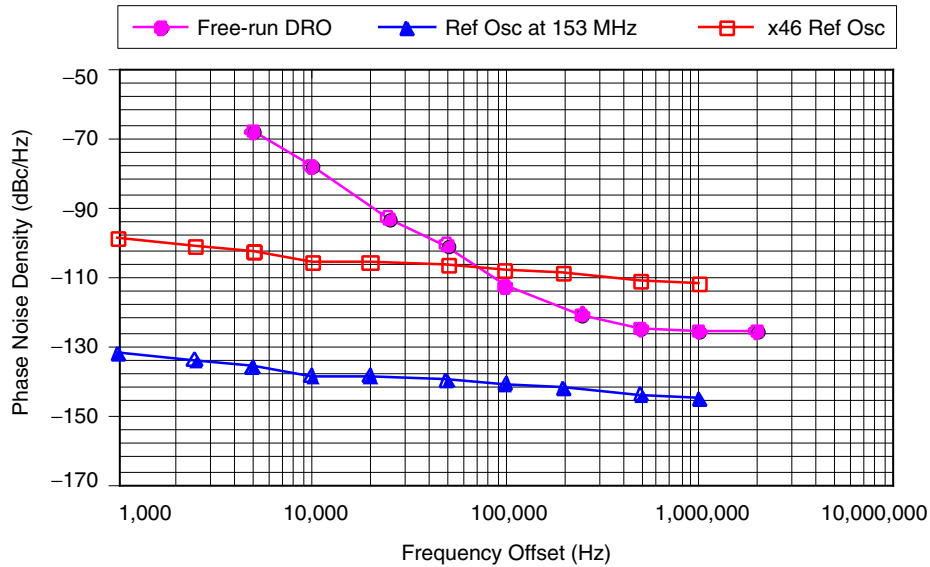

Fig. 26. Phase noise spectral density measurements of the free-running DRO and the reference oscillator. The open squares represent a calculation of the phase noise performance of the x46 reference that actually samples the DRO frequency in the SPD.
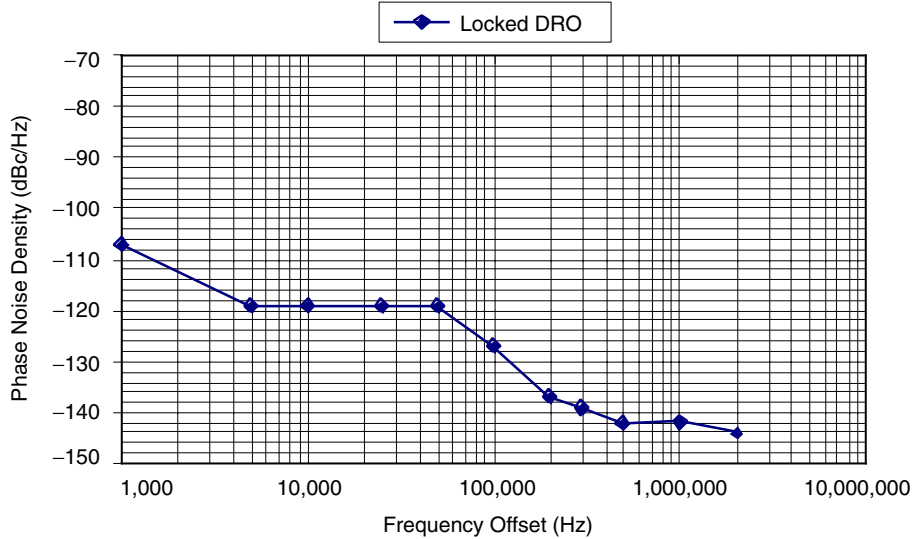
Fig. 27. Phase noise performance of the DRO locked via a first-order loop of about 50-kHz bandwidth to the 46th harmonic of the 153-MHz reference signal generated by the HP 8663 frequency synthesizer.

the loop bandwidth. The absolute value of the phase noise spectral density is not quite consistent with that expected based on the measurements of the individual components of the loop. Systematic errors in the measurements will have to be investigated in more detail to understand the inconsistencies at the 7- to 10-dB level.

From the measured data, the DRO is performing well with respect to the required phase noise performance of -90 dBc/Hz at 1 kHz and 100 kHz and -120 dBc/Hz at a 1-MHz offset. Of course, we have not yet introduced into the loop the NCO tuning signal, which could have a significant effect on the phase noise. We require some further breadboard development of the digital reference, as discussed above, before we can make the required measurements.

VIII. Future Work

In fiscal years (FYs) 2004 and 2005, we plan to continue with the development of the Advanced Transponder with the goal of achieving a prototype laboratory transponder that we can use to demonstrate key functionality and compatibility with the Deep Space Network using the Development and Test Facility.

In FY'04, we will continue with the detailed digital design of the tracking loop, the command detector, the downlink synthesizer, QPSK modulator, and turbo encoder, and we will investigate the possibility of including a low-density parity-check (LDPC) downlink encoder as well. We will continue to improve the fidelity of our breadboard prototype demonstration and complete the evaluation of our DRO-PLL tunable-frequency architecture.

IX. Conclusion

We have made significant progress during FY'03 in the development of an architecture and a signal-processing design for a new Advanced Deep Space Transponder. We have worked out a number of novel architectures for the functional blocks that allow for increased functionality and performance enhancements, and which should lead to simpler and lower-cost production when this transponder is developed as flight hardware. We have developed breadboard components, which we have used to demonstrate the feasibility of key architectural decisions, and we have begun to evaluate critical performance specifications

such as phase noise performance of the DRO-PLL receiver tracking and downlink synthesis loops. We have also generated a set of detailed specifications for radio frequency integrated circuits that we would like to see developed for application to this transponder architecture as well as to other ongoing and future radio technology development areas.

We will continue to pursue this development within the research and technology development program with the goals of delivering a prototype transponder demonstration and gaining support for the development of an engineering model and eventual flight unit to support missions launching in the 2010 time frame and beyond.

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